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MODEL CS-3,1

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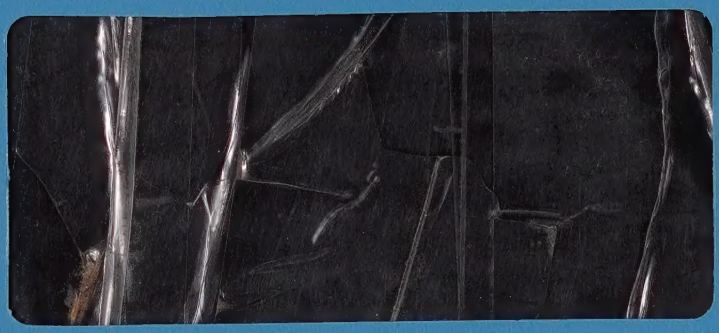

# DIGITAL VOLTMETER

## MODEL CS-3,1

## INSTRUCTION MANUAL

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# 1. SPECIFICATIONS

RANGE:

D. C. voltages from ±.001 to ±999 volts in ranges of ±.999/9.99/99.9/999 volts full scale. Voltages greater than 100 millivolts are displayed with three significant digits.

ACCURACY:

Within ±0.1% of reading ±1 count.

INPUT IMPEDANCE:

10 Megohms for D.C. on all ranges except the lowest range where it is a minimum of 1000 Megohms for D.C. (1 Meg in series with 0.1 mfd for AC).

FLOATING DIFFERENTIAL INPUT:

Truly floating and guarded differential input circuit permits differential voltage measurements with GUARD floating up to ±500 volts D.C. with respect to chassis, which is at power line ground.

COMMON MODE REJECTION:

1) With respect to power ground (GUARD and "LOW" input terminal connected together): For balanced or unbalanced (1000 ohm) D.C. common mode signals up to ±500 volts, and AC common mode signals up to 60 cps at 100 volts peak-to-peak maximum, the rejection is beyond the sensitivity of the instrument (greater than 100 db).

2) For truly differential inputs: (GUARD at the common mode potential with respect to "LOW" input terminal): Common mode error is plus 1 count or minus 1 count per 7 volts of D.C. common mode signal depending on polarity of GUARD relative to "LOW" terminal. The common mode potential between GUARD and "LOW" terminals is not to exceed ±100 volts.

RANGE SELECTION:

Automatic. A "HOLD" control disables the automatic down-ranging programmer

and permits manual selection of range if desired.

POLARITY INDICATOR:

Automatic.

BALANCING TIME:

0.15 seconds to 3.15 seconds, depending on the change of range required.

SAMPLE RATE:

One reading per second, (0.15 seconds conversion time and 0.85 seconds readout time), if no range change. Sample rate may be controlled externally in instruments provided with an output connector for printer.

EXTERNAL CONTROLS:

A five position switch provides the following functions: 1) "OFF"; 2) "AUTO" (for fully automatic operation); 3) "ZERO" (for checking zero: set by an externally available control); 4) "HOLD" (for manual range selection: disables the down-ranging programmer); 5) "CALIBRATE" (for checking absolute accuracy: set by an externally available control). The manual selection of range is accomplished by use of the "ZERO", "HOLD" and "CALIBRATE" positions.

OUTPUTS:

Available with ten line decimal coded output for digital print-out, or remote read-out at extra cost.

READOUT:

Long life standard size Nixie[1] tubes; readable at 30 feet.

INPUT CONNECTIONS:

Front and rear.

DIMENSIONS:

6 1/2 inches wide; 5 inches high; 8 3/4 inches deep. One or two units can be mounted in 5 1/4" standard rack panel without requiring modifications or any additional hardware.

---

[1] "Nixie" is a registered trade mark of the Burroughs Corporation.

CONSTRUCTION:

Completely solid state electronic circuitry except for two minature nuvistor tubes. Long life dry-reed relays for automatic ranging, polarity logic and amplifiers stabilization.

POWER:

105 to 125 volts or 215 to 245 volts AC: 50 to 60 cps; 17 watts.

## II. PRELIMINARY INSTRUCTIONS

### POWER REQUIREMENTS:

This instrument will operate either from a 115 ± 10 volts a.c. or a 230 ± 20 volts a.c. 50 to 60 cps. power source depending on the connection of the primary windings of the power transformer.

The instrument requires approximately 17 watts at either 105 to 125 V.A.C. or 210 to 250 V.A.C. 50 to 60 cycles per second. It is normally shipped wired for 105 to 125 V operation. If it is shipped wired for 210 to 250V operation the line cord will bear a tag at the plug end so marked. Transformer primary connections for both 115 volt and 230 volt operation are shown in Figure 1A and 1B respectively.

When it is necessary to operate the instrument at a different a.c. voltage than that wired for at the factory, the necessary changes on the transformer primary connections may be made by following the procedure outlined below:

1. Remove the cover by taking out the four screws at the back of the instrument. This will allow the cover to slide back.

2. Remove all plug-in boards from the instrument by pulling on the tabs protruding from each board through the sides of the guard chassis.

NOTE: The board carrying the counter and read-out assembly will not come out vertically. It is pulled vertically only enough to disengage it from the connector on the mother board, then it must be tilted back to clear the front panel as it is removed.

3. Locate the five screws on the face of mother board which secure it to the chassis and remove them.

4. Remove the knob from the selector switch.

5. Unsolder the connections to the input receptacle and remove the front panel by taking out the four screws securing it to the sides of the guard chassis.

6. Tilt the mother board up and connect the transformer primary as desired following the diagrams of Figure 1.

7. Reassemble the instrument following the above procedure in the reverse order.

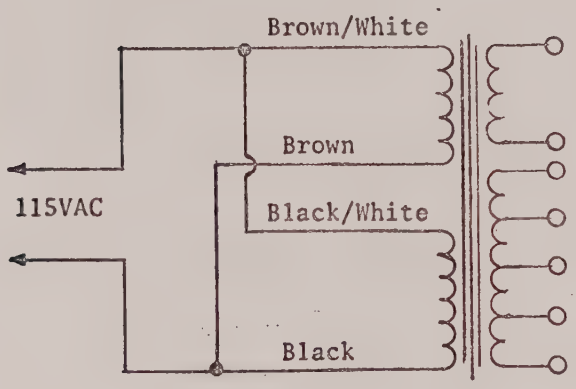



FIGURE 1A
115VAC Operation

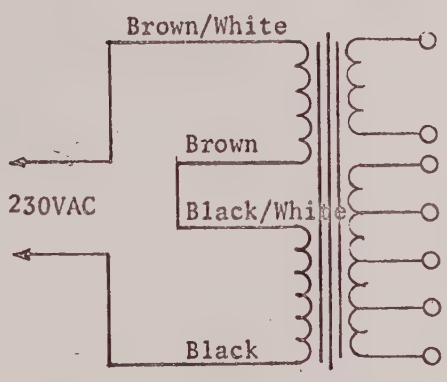



FIGURE 1B
230VAC Operation

FIGURE 1
TRANSFORMER PRIMARY CONNECTIONS

NOTE: The transformer primary windings are terminated on stand-off terminals located on the bottom of the MOTHER BOARD next to the transformer.

COOLING:

This instrument dissipates approximately 17 watts of power, the resulting heat being carried away by the free circulation of air through the ventilation holes in the cover.

To avoid overheating, care must be taken so that nothing is placed directly on top of the cover, and that there is at least 1/2 inch clearance between either

side or the bottom of the cover and any other solid object.

FUSING:

The primary of the transformer is fused with a standard 3 AG 1/4 amp. 250V Slo-Blo type fuse which gives adequate protection to the instrument in either 115V or 230V operation at either 50 or 60 cps. The fuseholder is accessible through the bottom of the instrument.

WARM-UP:

Because of the two tubes in the comparator circuit, approximately 15 minutes of warm-up time is required before the digital voltmeter will operate within its specified accuracy.

PANEL MOUNTING:

No additional hardware is necessary to mount this instrument on a 5 1/4" standard rack panel. Follow the procedure outlined below:

1. Cut an opening in the panel as indicated in Figure 2, on the next page.

2. Remove the cover from the instrument by taking out the four screws at the back and sliding it off horizontally.

3. Insert the instrument into the opening in the panel from the front, and reassemble the cover with the panel between the bezel and the front edge of the cover.

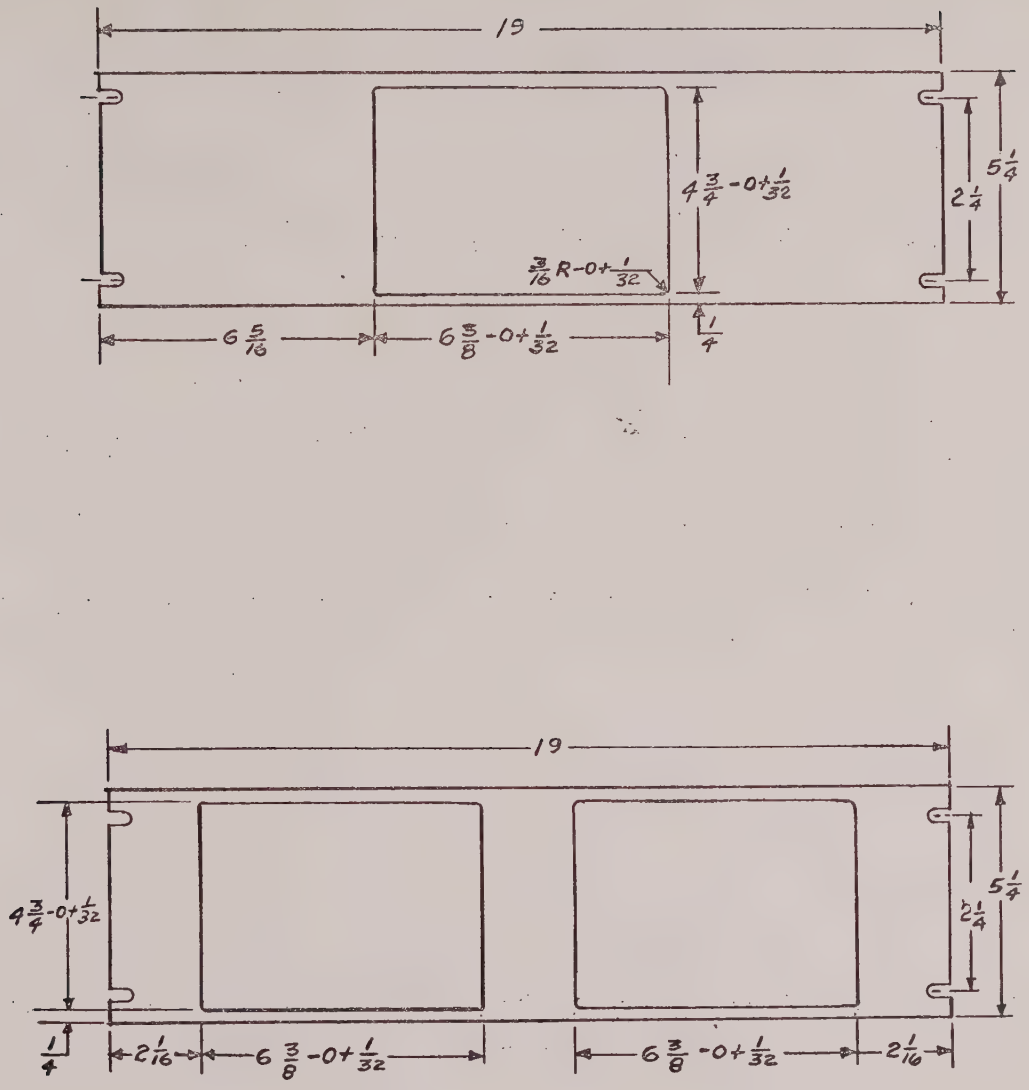



FIGURE 2

PANEL MOUNTING FOR CS-3.1 DIGITAL VOLTMETER

## III. OPERATING INSTRUCTIONS

### SELECTOR SWITCH FUNCTIONS:

The five position selector switch on the front panel permits the selection of the following modes of operation.

### AUTOMATIC:

With the switch in the "AUTO" position, fully automatic operation results. In this mode of operation any input voltage between 1 millivolt and 999 volts D.C. is displayed with the decimal point automatically appearing in the proper place. The polarity is also displayed automatically. For input voltages greater than 100 millivolts the attenuator programmer will always switch in a range for which a three digit number is displayed.

At the border line of any two ranges, for example, between 99.9 and 100 volts, the upper range will be switched in when the input increases from 99.9 to 100 volts or by 0.1 volt. However, when the voltmeter is in the upper range a decrease of 1 volt in the input signal is required to result in switching from the higher to the lower range. This is true because the resolution of the instrument is always one digit in the last place. Therefore, to measure such voltages with greater accuracy it is suggested that the selector switch be switched for one or more conversion cycles to the "ZERO" position and then back to "AUTO". This will force the attenuator programmer to first down-range then up-range to the required reading thus assuring highest resolution.

### ZERO

The "ZERO" position of the selector switch provides for the checking of the zero reference level of the voltmeter. With the switch in the "ZERO" position the reading should be .000 . The plus and minus signs will change alternately at the rate of the read-out frequency which is approximately 1 cycle per second.

In case the .000 reading is not obtained, refer to section V of this manual entitled "ADJUSTMENTS AND CALIBRATION" and follow instructions therein under the heading "ZERO LEVEL ADJUSTMENT".

MANUAL RANGE SELECTION (HOLD):

With the selector switch in the "HOLD" position, the down-ranging programmer is disabled. In this mode of operation the voltmeter will stay in the range corresponding to the input voltage at the time of switching from the "AUTO" position to the "HOLD" position as long as the input voltage does not increase enough to call for the next higher range. Decrease in the input voltage will not result in a change of range.

Setting the range higher than that called for by the level of the input voltage is possible by switching from "HOLD" to "CAL". While the decimal point is advancing up-range the desired range may be selected by going back to the "HOLD" position right after the decimal point has appeared at the desired place.

In a similar way any lower range may be switched in and held by going first to the "ZERO" position and then to the "HOLD" position when the decimal point gets to the desired place.

Since the up-ranging programmer is never disabled, it is impossible to switch to a range lower than that called for by the input voltage.

Successive measurements of voltages which fall within one attenuator range may be accomplished faster with the selector switch in the "HOLD" position, since in this mode the attenuator will not return to its lowest range each time the probes are disconnected from the point of measurement.

CALIBRATE:

In this position of the selector switch the read-out should be the same as the calibration number appearing in the lower left hand corner of the read-out window. In the event the read-out is different than the calibration number refer to section V of this manual entitled "ADJUSTMENTS AND CALIBRATION" under

the heading "CALIBRATION ADJUSTMENT".

OFF:

In this position the primary of the power transformer is disconnected from the power source. The switch should be in this position when the instrument is not in use.

THE PROBE:

Two receptacles are provided for the probe, one on the front panel and one at the back of the instrument. The probe may be plugged into either of them by inserting the plug into the receptacle and turning the lock spring to secure it in place.

The probe is terminated in three banana plugs which are pluged into alligator clips. The functions of the three leads are as follows; The red terminal is the "HIGH" input to the attenuator. The black one is the "LOW" input. The yellow terminal is connected to the "GUARD" circuit, and for all ordinary measurements not requiring the truly floating differential input, the yellow and black leads should be connected together.

The voltmeter will display a positive sign when the "HIGH" input terminal is positive with respect to the "LOW" input terminal. When the reverse is true a minus sign will be displayed.

MEASURING DC VOLTAGES:

Any DC voltage between 1 millivolt and 999 volts may be measured by this instrument within the specified accuracy. Two types of measurements will be discussed. The first type of measurement will be referred to as DIFFERENTIAL and the second type of measurement will be referred to as DIFFERENTIAL WITH FLOATING INPUT.

DIFFERENTIAL MEASUREMENT:

This type of measurement assures the best accuracy with a D.C. common mode rejection beyond the sensitivity of the instrument.

To measure the unknown potential connect the "HIGH" and "LOW" terminals of the probe across it, keeping the "GUARD" and "LOW" terminals of the probe together, and set the selector switch in the "AUTO" position.

CAUTION: MAXIMUM ALLOWABLE POTENTIAL BETWEEN THE "GUARD" AND CHASSIS GROUND IS $\pm$ 500V.

The proper range will now be established automatically and the readout will present a three digit number, if the unknown voltage is greater than 100 millivolts. If manual range selection is desired it may be obtained by using the "HOLD" position as described previously (see "MANUAL RANGE SELECTION" above).

An input voltage may be applied with the selector switch in any position. However, when switching from "ZERO" to "CAL" positions, with an input voltage applied to the instrument the switch must be left momentarily in the "HOLD" position for a time long enough to allow the decimal point to advance and stop in the proper place, after which the "CAL" position may be switched in. When this procedure is not followed as described above the attenuator may not be switched properly (dependent on the input voltage level) and an incorrect calibration readout will be displayed. This is due to timing sequences associated with the attenuator programmer and up-ranging logic circuits and does not indicate any malfunctioning of the instrument. In case of an incorrect calibration reading the decimal point will not appear as it should, to the right of the least significant digit. Such a reading with the selector switch in the "CAL" position will indicate that the above discussed switching precautions where not taken.

DIFFERENTIAL MEASUREMENT WITH FLOATING INPUT:

A truly floating differential input is obtained when the "GUARD" terminal is disconnected from the "LOW" input terminal and placed at some other potential level. Now only the "HIGH" and "LOW" inputs are connected across the unknown

potential. Internally these two terminals are only connected to the attenuator which is completely isolated from the rest of the instrument. The difference between this type of measurement and the one described under DIFFERENTIAL MEASUREMENT is that with the "GUARD" circuit disconnected from the attenuator input, minimum coupling exists between the voltmeter input and the power line.

To measure an unknown potential with FLOATING INPUT connect the "HIGH" and "LOW" terminals of the probe across the potential to be measured. The "GUARD" terminal should be connected to some point whose potential is close to that of the "LOW" terminal. If such a point is not available connect the "GUARD" terminal to ground.

CAUTION: (THE POTENTIAL BETWEEN THE "GUARD" TERMINAL AND THE "LOW" TERMINAL IS NOT TO EXCEED ± 100 VOLTS.)

Under these conditions the reading will be in error by an amount proportional to the common mode voltage, being defined as the voltage between the "LOW" input terminal and the "GUARD" terminal. This error amounts to about one count (±) for each (±) 7v of common mode voltage.

If manual range selection is desired it may be obtained by using the "HOLD" position as previously described (see "MANUAL RANGE SELECTION" above).

DIGITAL OUTPUTS:

The digital output signals of the CS-3.1 Digital Voltmeter are brought out to a connector mounted on the rear of the instrument. The Printer Connector Chart, Figure 3, on page 15 identifies the connector contacts. These outputs may be used to drive any digital printer or a remote read-out unit with ten line decimal data entry whose inputs do not require more than 2 milliamps of current per line to enter the data. Notes following the Printer Connector Chart on page 15 specify the maximum "ON" and "OFF" loading conditions of the voltmeter outputs.

PRINTER: The following two commercially available digital printers are suitable for operation with the CS-3.1 Digital Voltmeter.

1) Beckman Instruments, Inc.
   Model 1453 Digital Printer.

2) Hewlett Packard
   Model 562A Digital Recorder.

When ordering either of the above instruments for operation with the CS-3.1 digital voltmeter, the following options should be specified.

1) Input Code: 10 line decimal.

2) Input signal polarity: The digital data entry circuit boards (column boards) must have negative inputs ("1" state negative).

3) Special characters:
   a) Plus and minus signs.
   b) Four characters to indicate the decimal point information.

The interconnections between the CS-3.1 digital voltmeter and a printer depends on the type of printer used. To use the Beckman Instruments printer refer to the Printer Connector Chart on page 15 of this manual. Also refer to the Beckman Instruments Printer Manual and find the ten line input cable schematic diagram. To interconnect the two instruments, a semiconductor junction diode having at least 200 volts reverse breakdown rating must be used as a coupling element in each signal line. The cathode ends of all diodes must connect to the digital voltmeter outputs, and the anode ends to the printer inputs. The print command pulse must also be coupled through a semiconductor diode.

To provide proper "ON" and "OFF" levels for signals entering the printer, its signal ground must be connected to the +24 volt supply of the digital voltmeter.

The common mode rejection of the CS-3.1 digital voltmeter when connected to operate a digital printer will be degraded somewhat when differential measurements are made because the guard circuit of the digital voltmeter will now be connected through the power supply to the printer circuits which are not very

well isolated from the power line. Also the maximum D.C. common mode voltage between the GUARD terminal of the voltmeter and the power line ground will be only ±100 volts as specified for the internal ground of the Beckman Printer. In this mode of operation, the best results will be obtained with the "GUARD" and "LOW" terminal of the digital voltmeter connected to the power line ground.

Output to input connections for the Hewlett Packard Printer are the same as for the Beckman Printer except for the following:

1) Connect the CS-3.1 digital voltmeter signal ground to the reference voltage input of the Hewlett-Packard Printer.

2) The print command pulse coming out of the voltmeter with +24 volts amplitude and approximately 150 millisecond duration must be reshaped as follows before its application to the printer. Use a differentiator circuit to obtain an output pulse of at least 20 microseconds in width. Clamp the positive at ground level and use only the negative going pulse as a print command signal.

All of the limitations in operation of CS-3.1 digital voltmeter with the Beckman Printer also apply here, except of the D.C. common mode voltage with respect to power line ground, which with this printer is ±150 volts.

WINCHESTER MRE 50S-J

| CONTACT | OUTPUT FUNCTION | | CONTACT | OUTPUT FUNCTION | | CONTACT | OUTPUT FUNCTION |
|---|---|---|---|---|---|---|---|
| B | Minus Sign | Shield 1 | W | 9 Second Digit | Shield 3 | HH | Open |
| F | Plus Sign | | A | 0 First Digit | | AA | Open |
| L | 0 Third Digit | | E | 1 First Digit | | EE | Open |
| R | 1 Third Digit | | K | 2 First Digit | | x | Open |
| V | 2 Third Digit | | P | 3 First Digit | | BB | Open |
| Z | 3 Third Digit | | U | 4 First Digit | Shield 4 | FF | Open |
| d | 4 Third Digit | Shield 2 | Y | 5 First Digit | | z | Open |
| j | 5 Third Digit | | c | 6 First Digit | | | |
| p | 6 Third Digit | | h | 7 First Digit | | | |
| u | 7 Third Digit | | n | 8 First Digit | | | |
| y | 8 Third Digit | | t | 9 First Digit | | | |
| CC | 9 Third Digit | | C | 10 Multiplier | | | |
| D | 0 Second Digit | | H | $10^1$ Multiplier | Shield 5 | | |
| J | 1 Second Digit | | M | $10^2$ Multiplier | | | |
| N | 2 Second Digit | | S | $10^3$ Multiplier | | | |
| T | 3 Second Digit | | W | Signal Ground | | | |
| X | 4 Second Digit | Shield 3 | a | 200V Supply | | | |
| b | 5 Second Digit | | e | 24V Supply | | | |
| f | 6 Second Digit | | k | Inhibit input, "I"-Shield 6 | | | |
| m | 7 Second Digit | | r | Master Timer, "T"--Shield 7 | | | |
| s | 8 Second Digit | | v | Print Command------Shield 8 | | | |
| | | | DD | 120 cps Signal-----Shield 9 | | | |

FIGURE 3

PRINTER CONNECTOR CHART

NOTES:

1) Signal levels of all decimal outputs are as follows: +5 volts when "ON", +100 to +200 volts when "OFF".

2) Signal levels of plus and minus sign are +.5 volts when "ON", +100 to +200 volts when "OFF".

3) Multiplier outputs are +.5 when "ON" and +24 to +30 volts when "OFF."

4) Master Timer Signal, T:

-4 volts during conversion period.
+7 volts during display period.

5) Maximum load for any signal when "ON" is 5 milliamp. Maximum load for any signal in the "OFF" condition is 100 ua. Master timer may be continuously loaded with 2 ma. Maximum capacitive load is 1000 picofarads for any signal line. Maximum of 6 ma may be drawn out of the 24 volt and the 200 volt supplies.

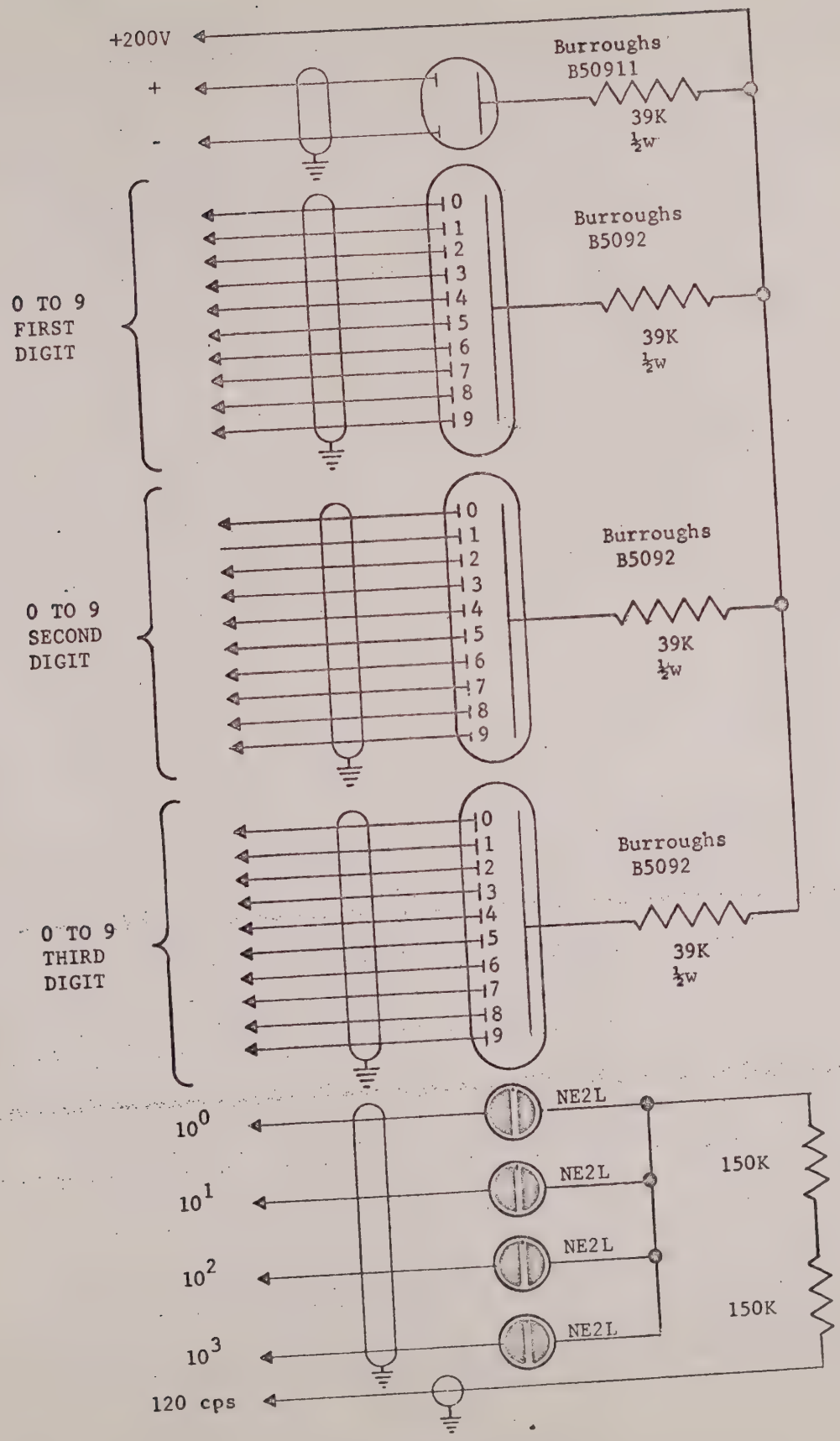
6) Use a multiconductor shielded cable to wire the mating connector. Groups to be shielded are shown in Figure 3.

REMOTE READ-OUT: The digital outputs brought out to the printer connector may also be used to drive a remote read-out unit having a 10 line parallel decimal input. The Printer Connector Chart is shown on page 15. Maximum load for each output is specified in the notes below the chart. When the read-out device demands more output current than the maximum value specified, a series of buffer amplifiers must be used between the voltmeter outputs and the input to the read-out unit. Such an arrangement, however, is not recommended because connection of buffer amplifiers to an external power supply will result in degradation of the common mode rejection characteristic of the instrument.

The best performance will be achieved with a passive read-out device connected directly to the voltmeter outputs and operated by the voltmeter power supply. A remote read-out unit using gas discharge tubes for the numeric presentation of data is best suited for this application. This type of read-out is used in the voltmeter itself, and since the output impedance of the driving stages is sufficiently low, two of such read-out units may be operated in parallel. The schematic diagram on page 17 shows the remote read-out unit and its connections to the voltmeter outputs. The specified components are identical with those used in the internal read-out of the CS-3.1 digital voltmeter.

The 32 digital outputs (plus-minus sign and three decimal digits) brought out to the output connector are internally connected to the nixie tube cathodes. Connecting the cathodes of the remote read-out tubes directly to the voltmeter outputs will result in a simultaneous read-out of data on both units. This also holds true for the multiplier outputs.

The principle of operation of the decade counter and the visual display is discussed under the heading of "Counter" on page 27. It may be found helpful to read this section of the manual before connecting and operating a remote read-out unit.




REMOTE READ-OUT UNIT

READ ON COMMAND: Instruments provided with the output connector for printer may be controlled externally to read and display on command. If this mode of operation is desired refer to the Printer Connector Chart, Figure 3, and locate points "T" and "I". "T" is the master timer output and "I" is the inhibit signal. Connecting "T" and "I" together will cause the instrument to display its last count as long as the two points stay connected. Opening the connection between "T" and "I" will permit the instrument to recycle in its normal mode until this connection is made again.

If a single conversion is desired, the connection between the two points should be broken for a period of at least 100 milliseconds but not more than 500 milliseconds and then restored. The instrument will then execute a complete conversion cycle and hold the result until the connection is broken again.

The open circuit voltage between terminals "T" and "I" is approximately 12 volts and a current of about 250 microamps flows when the connection is closed.

It is important that the relay contacts used to make and break the connection be well isolated from power ground and from the instrument's signal ground as well. If the instrument is to be used floating, these contacts must be capable of floating ±500 volts with respect to ground.

## IV. DESCRIPTION OF CIRCUITS

### PRINCIPLE OF OPERATION:

The Model CS-3.1 Digital Voltmeter operates by comparing the voltage being measured with an internally generated staircase. The staircase is generated by a "charge pump" circuit driving a Miller integrator. The charge pump is driven by a 10KC oscillator which also drives a three digit decade counter. A series of charge pulses is applied to the integrator input, their amplitude being adjusted so that each pulse changes the integrator output by 1 mV. Thus, at any instant, the accumulated count in the counter represents the staircase level in millivolts.

The voltage being measured is applied to an attenuator whose attenuation ratio is automatically set to make its output lie between zero and one volt for any input voltage from zero to one thousand. Once each balancing cycle a sample capacitor is switched across the attenuator output and held there for a time sufficient to allow it to charge to the attenuator output voltage. This capacitor is then switched to the input of a comparator circuit which gates off the internal oscillator when the staircase voltage equals the voltage on the capacitor. Thus, the counter reading at this point is numerically equal to the charge on the sampling capacitor in mV, and with an appropriate multiplying factor (indicated by the automatically positioned decimal point in the display) to the voltage being measured.

### DESCRIPTION OF CIRCUIT FUNCTIONS:

A functional block diagram of the complete voltmeter is shown in PAR Dwg. No. 0188-C-SD. The function of each circuit shown will now be described:

1. The ATTENUATOR circuit consist of four precision resistors R909, R910, R911 and R912, which are switched in various combinations by relays A, B, C, D and D' to produce a voltage across the sampling capacitor, C901 which is always

less than, or equal to, 999 millivolts for all inputs between 1 volt and 999 volts. On the lowest range, that is for inputs between 0 and 999 millivolts, the voltage on the memory capacitor equals the input voltage. The three 75 volt neon lamps shown serve to limit the sampling capacitor voltage before the proper range is established. Switches shown schematically represent contacts of the front panel selector switch.

2. The sampling circuit consisting of the sampling capacitor C901 and six high reliability magnetic reed-relay contacts, takes a sample of the input voltage during every readout cycle. This is done by closing the two E1 contacts which connect the sampling capacitors across the attenuator output during the 0.85 second readout time. At the end of this period contacts E1 open and the analog to digital conversion begins after contacts F2 and F4 or G2 and G4 close, (depending on polarity) connecting the memory capacitor between the output of the integrator and the input of the comparator. At the end of the conversion cycle all contacts open and then E1 contacts close again. This cycle repeats with the specified conversion and readout periods which are approximately 0.15 and 0.85 seconds respectively.

3. The three blocks marked INTEGRATOR, CHARGE PUMP and MASTER OSCILLATOR comprise the SYNCHRONOUS RAMP GENERATOR circuit, which derives its name from the fact that the millivolt steps of the ramp are generated synchronously with the MASTER OSCILLATOR frequency. The integrator amplifier is stabilized before each conversion cycle by means of a negative feedback loop switched in by reed relay contacts E3. When the E3 contacts open shortly before the conversion begins, the INTEGRATOR output is essentially at ground level. The MASTER OSCILLATOR is started at the beginning of the conversion cycle. It drives both the "charge pump" and the three digit decade counter simultaneously; so that each step of the ramp is counted. Since each ramp step is exactly one millivolt high, the accumulated count represents the instantaneous ramp level in millivolts. The

complete analog to digital conversion process is explained in a separate paragraph following the description of the comparator.

4. The COMPARATOR is a differential amplifier with very high input impedance. One input (in phase with the output) is used as a zero-crossing detector. The other input is used to stabilize the circuit before each conversion cycle by means of a negative feedback loop through contacts E1. Another stabilizing contact pair E3 grounds the comparator input. The output of the comparator is fed to the OSCILLATOR GATE and to the POLARITY SENSING LOGIC.

5. The process of analog to digital conversion consists of a number of events programmed by the RELAY SEQUENCE PROGRAMMER. These are as follows:

A. Upon a command from the MASTER TIMER, the counter is reset to 000 and all E1 contacts open. This disconnects the sampling capacitor from the attenuator circuit and opens the stabilizing feedback loop of the comparator.

B. Approximately two millisecond later either F2 or G2 closes, depending on the state of POLARITY SENSING LOGIC.

C. A few milliseconds later stabilizing contacts E3 open.

D. After a few milliseconds time delay, F4 closes if F2 was closed, G4 closes if G2 was closed.

E. For the right polarity, the comparator output is negative. The wrong polarity will be marked by the comparator output going positive when F4 or G4 closes. This positive pulse will be sensed by the POLARITY SENSING LOGIC whose output signals the RELAY SEQUENCE PROGRAMMER to change the closures of F and G contacts, thus reversing the polarity of the sampling capacitor. At the same time the polarity sign on the display is also changed.

F. At the end of the polarity sensing cycle the sampling capacitor

will have its positive terminal connected to the ramp generator output (initially at ground) and its negative terminal connected to the COMPARATOR input. The COMPARATOR input will thus be below ground by the voltage on the sampling capacitor.

G. Approximately 5 milliseconds after the G4 contact closes, the oscillator gate starts the MASTER OSCILLATOR. A staircase appears at the COMPARATOR input shifted in the negative direction by the voltage across the sampling capacitor. It is clear now that the COMPARATOR input will cross ground level at the point where the ramp voltage in millivolts, as recorded by the accumulated count, is equal to the voltage across the sampling capacitor. The COMPARATOR output goes positive immediately after the input crosses ground. At this point the OSCILLATOR GATE receives a signal to stop the MASTER OSCILLATOR. The state of the counter is displayed on the readout; the number representing millivolt count of the sampling capacitor voltage is related to the input voltage by a factor of 1, 10, 100 or 1000 depending on the range of attenuator, which is indicated by the decimal point in the visual display. The count is displayed for approximately 0.85 seconds.

H. At the beginning of the display time the MASTER TIMER resets the RELAY SEQUENCE PROGRAMMER, which causes all F and G contacts to open and E1 as well as E3 contacts to close again. The amplifiers are now stabilized and the sampling capacitor takes another sample of the input voltage. After 0.85 seconds the MASTER TIMER initiates another conversion cycle. The timing chart Figure 4 shows the phase relations as well as the amplitudes and time durations of various waveforms discussed above.

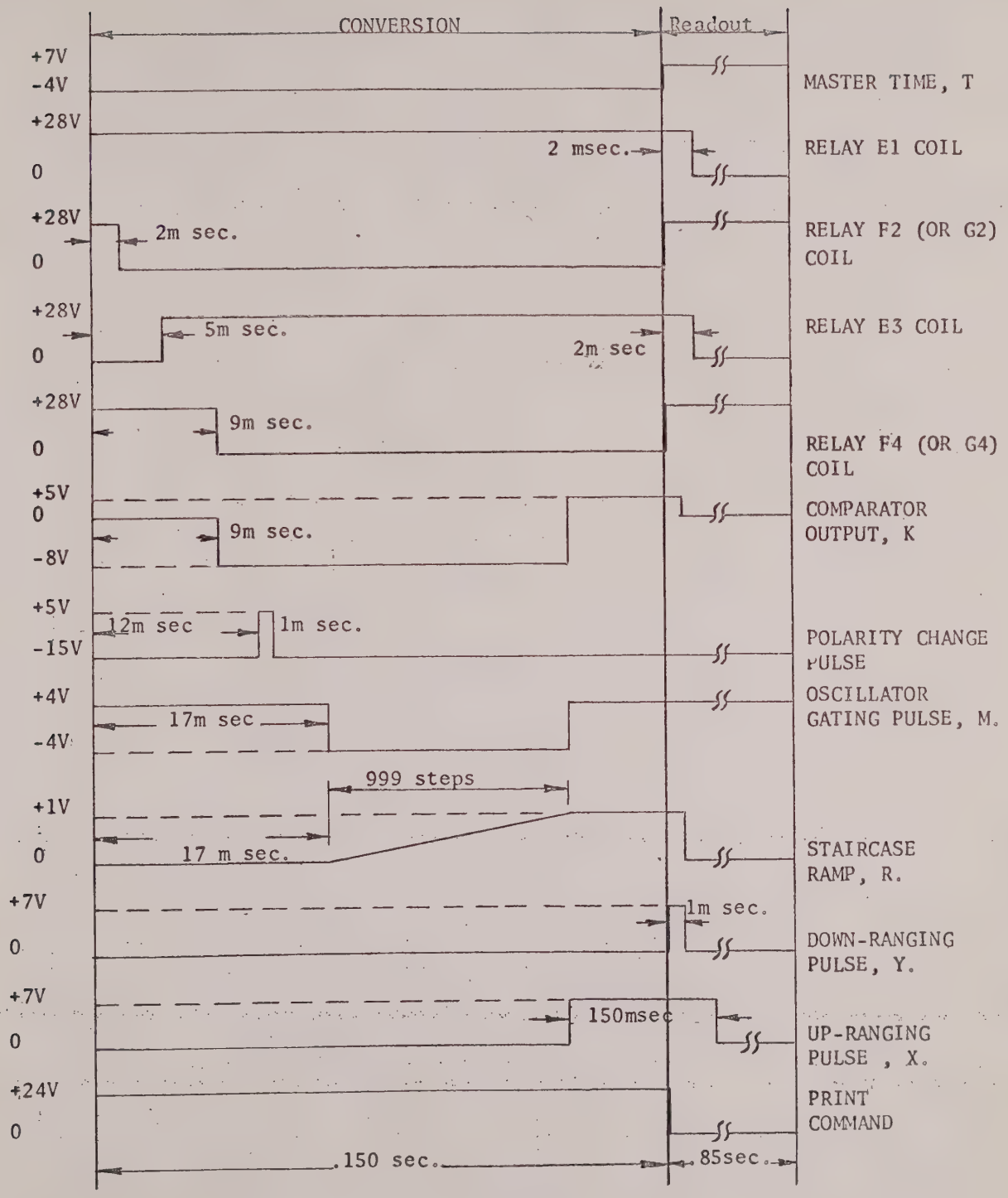



FIGURE 4

TIMING CHART

6. To complete the functional description of circuits the automatic ranging process will now be described. Let us assume first that the attenuator is in its 1:1 range when a voltage is applied calling for the 1000:1 range. The automatic up-ranging cycle is initiated as follows: The sampling capacitor being charged to a voltage higher than 999 millivolts will cause the three digit decade counter to go through its full capacity count of 999 and to start a new count beginning at 000 again. The UP-RANGING LOGIC CIRCUIT senses the number "9" going off in the most significant digit and signals the ATTENUATOR PROGRAMMER to switch to the next higher attenuator ratio, in this case the 10:1. The attenuator output is sampled again and since it is still too high the 100:1 attenuator ratio will be switched in. This process repeats until the voltage on the sampling capacitor is 999 millivolts or less (i.e. 1000:1 attenuator ratio in this example). This attenuator range will now stay switched in unless the input voltage changes enough to call for another range. For inputs higher than 999 volts the up-ranging cycle will continue since a balance cannot be achieved for such a voltage. In such a case the decimal point will continue to cycle through all four locations until the input voltage is reduced below 999V.

In a similar way the down-ranging program switches the attenuators from higher to lower ratios. This occurs when the input voltage is too low for the range and as a result the memory capacitor is charged to 99 or less millivolts. The DOWN-RANGING LOGIC senses zero in the most significant digit and signals the ATTENUATOR PROGRAMMER to switch in the next lower range. Again this process repeats with each conversion and readout cycle until the proper range is established. In the worst case the attenuator has to be switched three times to find a proper range and therefore the maximum ranging time is three seconds. (this applies both to up and down ranging)

The ATTENUATOR PROGRAMMER consists of two gated bi-stable multivibrators

and a transistor decoding matrix. It has two inputs and four outputs which drive the attenuator relays. The up-ranging signal feeds one input and the down-ranging signal feeds the other. The switching sequence: A to B, B to C, C to D results when the down ranging pulse is applied. For the up-ranging pulse the sequence is D to C, C to B and B to A. The circuit details of this programmer are explained under ATTENUATOR PROGRAMMER.

7. The POWER SUPPLY consisting of semi-conductor rectifiers and regulators provides the necessary voltages for the voltmeter system. The + 28 volt and the + 200 volt lines are not regulated. It is completely conventional in operation and does not require any further discussion.

CIRCUIT LOCATIONS:

The locations of the printed circuit boards in the chassis are shown in Figure 5. The four boards marked 1, 2, 3 and 4 comprise the COUNTER and VISUAL DISPLAY assembly. Note that only board No. 4 is plugged into the mother board; the other three are assembled to board #4 by means of connectors.

The boards are identified by numbers appearing on the printed circuit side of each board. For reference the board locations in the chassis are tabulated below:

Wiring of components on the MOTHER BOARD as well as the front and back input connector is shown in Dwg. No. 0386-B-SD.

Since some of the circuits are distributed on more than one board, it was convenient to arrange the circuit discussion given below on a circuit bases rather than by boards. The board location of each complete circuit or a part of circuit being discussed is clearly stated.

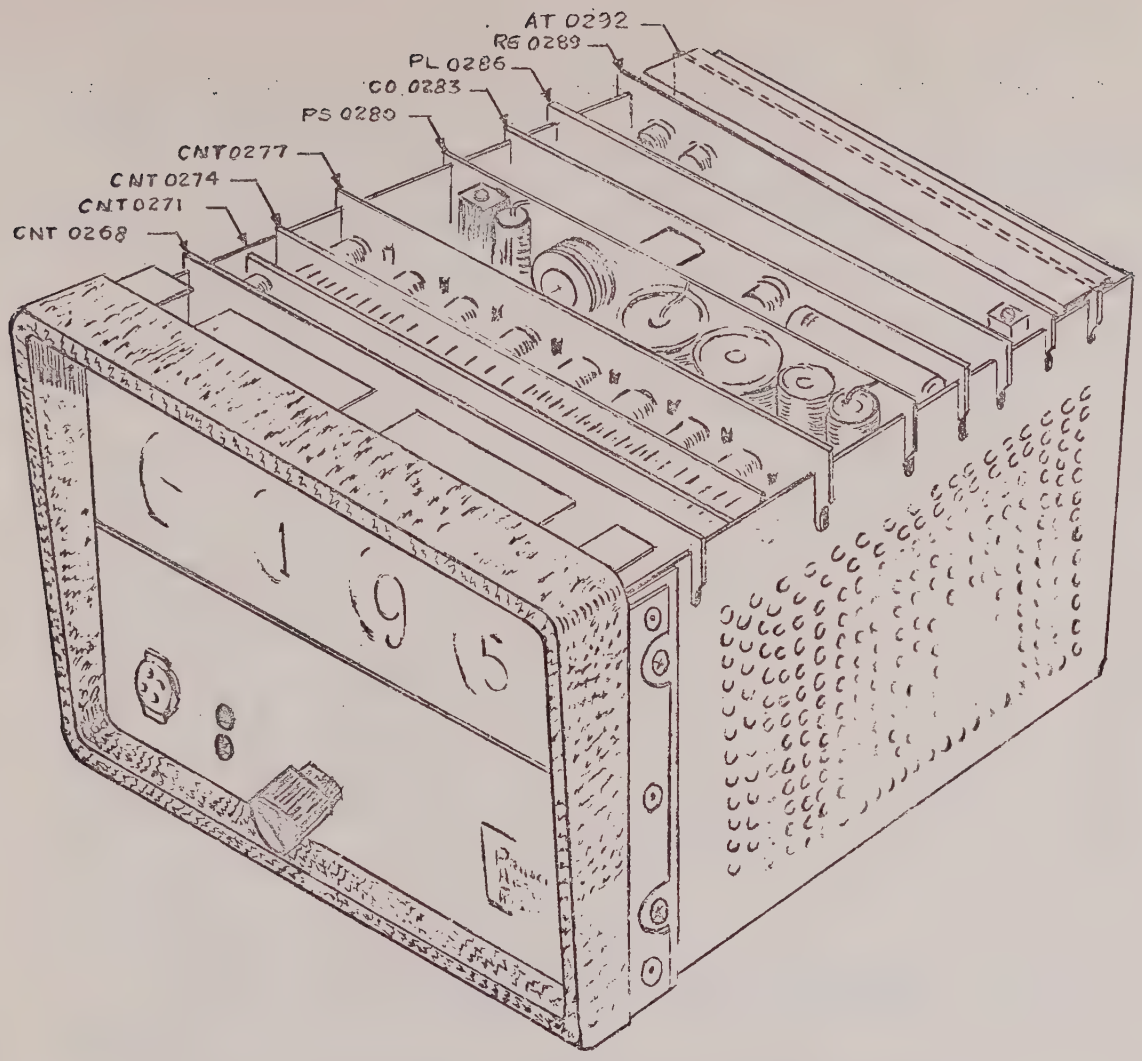



FIGURE 5

BOARD LOCATION TABLE

| BOARD NO. | NAME | LOCATION (numbered from front to back) | CIRCUIT DWG. NO. |
|---|---|---|---|
| CNT 0268 | Counter Board 1 | 1 | 0315-C-SD |
| CNT 0271 | Counter Board 2 | 2 | 0315-C-SD |
| CNT 0274 | Counter Board 3 | 3 | 0315-C-SD |
| CNT 0277 | Counter Board 4 | 4 | 0315-C-SD |
| PS 0280 | Power Supply | 5 | 0318-C-SD |
| CO 0283 | Comparator | 6 | 0136-C-SD |
| PL 0286 | Programmer Logic | 7 | 0135-C-SD |
| RG 0289 | Synchronous Ramp Generator | 8 | 0137-C-SD |
| AT 0292 | Attenuator | 9 | 0140-C-SD |

COUNTER:

The counter, including the VISUAL DISPLAY tubes and decimal point lights consists of four boards as listed in the BOARD LOCATION TABLE.

The circuit diagram of this assembly is shown in Dwg. No. 0315-C-SD. The printed circuit connectors which connect to the mother board are identified by numbers in the upper half of the circles appearing in a column at the left of the drawing. The numbers represent connectors looking at the component side of board No. 4 and counting from left to right. In the lower part of the circle the connector function is identified. In marking the components on the schematic the following system is used. A component is denoted by a letter followed by a 3 digit number. The letter identifies the type of component (R for resistor, C for capacitor, etc.) The first digit of the number represents the board number, (see table in Figure 5) the other being assigned serially to components of the given type on the board. The same system of component identification is used throughout the entire voltmeter.

Connectors interconnecting the four counter boards are not shown on the schematic.

The three digit decade counter consists of three ten stage ring counters. Each ring counter stage employs a complementary transistor pair in the hook connection. Since all three ring counters are identical, only the first stage will be described in detail.

All ten emitters of the PNP transistors are connected to a common point which is the collector of the driver transistor Q401. The emitters of all NPN transistors which drive the Nixie tubes are connected to a common point which is at a constant dc potential of + 5.2 volts. The emitter of Q403 supplies this voltage for all three counters. The base of each PNP transistor is returned through a 1K resistor to a dc potential of + 7.3 volts. This voltage is derived from the + 8 volts supply line by means of the forward drop across

diode D401. The base of each NPN transistor is connected through a 1K 5% resistor to ground. The voltage levels are chosen for the optimum forward and reverse bias conditions in the on and off state of both transistors.

The diodes serve to disconnect the collectors of the Nixie drivers on the positive swing so that the necessary 100 volt difference between the "on" and "off" cathodes is maintained. Capacitors between stages transfer the "on" condition from one stage to the next at the driving frequency.

To discuss the performance of the ring counter let us assume that the first stage (Q404 and Q424) has been reset to the "on" state. All other stages will necessarily be "off" because the value of resistor R405 (2.K, 5%) is chosen to supply only enough current for one stage to be "on". The oscillator waveform (essentially square-wave) arrives at the point marked OSC and after being differentiated drives the base of Q401. The time constant of the differentiator consisting of C403 and R404 is set so that Q401 turns "on" for approximately ten percent of the oscillator period. When the driver transistor Q401 momentarily turns "on", the PNP transistor of the "on" stage (in this case Q404) turns "off". This cuts off the base current to the Nixie driver Q424 which also turns "off". The current in resistor R431 previously supplied by the collector of Q404 is now replaced by the current from the coupling capacitor C406, which is also the current through resistor R412. The voltage developed across R412 causes the base of Q405 of the next stage to be at a lower voltage than the other nine bases. The value of the coupling capacitor is large enough to maintain this voltage until Q401 begins to turn "off" again driving all PNP transistor emitters positive. While the emitters are going positive the base-to-emitter junction of Q405 will become forward biased first which will cause stage two (Q405 and Q425) to turn "on". This process of transferring the "on" condition from one stage to the next repeats at the driving frequency. To form a decade ring counter the last stage

is coupled back to the first via capacitor C405.

The other two decades are identical in design and performance to the one just described except for the operating frequency. Each decade counter is driven by the output of the last stage (number 9) of the preceding decade. The Nixies are driven directly by counters.

A forced reset to 000 before each conversion is accomplished by means of the differentiated master timer complement pulse ($T^{\ell}$) arriving at the base of Q101. Diodes D101, D102 and D103 couple the collector of Q101 to the "zero" stage of each decade. When $T^{\ell}$ goes positive, Q101 turns "on" for a period set by the differentiator at its base (C101 and R105). The negative going collector of Q101 turns "on" all three "zero" stages, thus clearing the counter for the next conversion.

The circuits associated with the decimal point lights perform as follows: One electrode of each neon light is connected to a common point which through two series resistors R108 and R109 leads to a terminal marked T5. The other electrodes of lights B102, B103 and B104 are brought out to terminals marked B, C and D, which lead to collectors of the attenuator relay driver transistors located on the comparator board. The fourth light is driven by a logic circuit consisting of diodes D106, D107, D108 and an inverter Q102 whose collector drives B101. The collectors of the attenuator driver transistors as well as Q102 swing from ground to a maximum of + 28 volts. However because of the nature of the waveform at point T5 it is possible to drive the 75 volt neon lights "on" and "off" with this small potential difference. The T5 waveform is a full-wave rectified sinusoid obtained from the voltage doubler supplying the + 200 volt line. It swings from ground to + 200 volts and back to ground at twice the frequency of the power line. When it swings "up" it will always turn on that light whose other electrode is at the lowest voltage.

The (+) Nixie is driven by a logic circuit located on the programmer logic board. The driving signals arrive at the counter board via connectors marked plus (+) and minus (-).

POWER SUPPLY

The power supply transformer is mounted on the mother board. The rectifiers filter capacitors, and regulators are located on board number 5. The transformer wiring is shown on the mother board wiring schematic Dwg. No. 0386-C-SD. The circuits contained on board 5 are shown in Dwg. No. 0138-C-SD. The power supply provides four regulated voltages and two unregulated voltages. The minus fifteen (-15) volt supply and the plus twenty four (+24) volt supply are regulated by series transistor regulators Q504 and Q503 respectively. The plus eight (+8) volt line and the minus nine point three (-9.3) volt line are regulated by zener diodes D502 and D503 respectively.

Printed circuit connector numbers are shown in the circles at the left of the schematic. The connector functions are also indicated. Those starting with letter "T" go to the transformer secondary windings. Since all circuits contained on this board are completely conventional no further discussion is necessary.

COMPARATOR:

The COMPARATOR circuit occupies most of the central area of board number 6. The schematic diagram of this circuit is shown in the lower right hand corner of Dwg. No. 0136-C-SD. There are other circuits located on board 6 such as the UP-RANGING and DOWN-RANGING logic circuit, TRL matrix of the ATTENUATOR PROGRAMMER and some reed relay drivers. All these will be explained later when the logic gates and programmer are discussed.

The COMPARATOR circuit consist of three cascaded differential amplifier stages. Because of the high input impedance required, the input stage of the COMPARATOR employes two RCA nuvistor type triodes V601 and V602 connected as a

differential amplifier. The second stage consists of differential pair of transistors Q615 and Q616, whose emitter voltage is set by resistors R647 and R649 at the base of Q608. Diodes D617 and D618 limit the plate voltage swing of the nuvistor triodes in case of input overdrive. The last stage consists of Q617 and Q618. The emitter follower Q614 provides a single ended output, wired to connector number 12 marked "K".

The COMPARATOR circuit operates by detecting the zero crossing of the grid of V601, as already mentioned in the description of the block diagram. The grid of the other tube, V602, is grounded via C612.

During the stabilization time, negative feedback is applied to this point through R651 by means of relay contact closure between terminal 15 marked $E_1K$ and terminal 12 marked "K". Also at the same time grid of V601 is grounded through contact $E_3G$ at terminal 16. Capacitor C612 charges to the output level, which the negative feedback will force close to ground. When the feedback loop is open the comparator is stabilized and ready to operate. The memory capacitor C612 and filter capacitor C613 are both connected to signal ground "SG" at terminal 14.

The voltage gain of the comparator amplifier is approximately 5000. The frequency response ranges from D.C. to approximately 30KC which is sufficient to pass the 10KC staircase at the zero crossing point.

MASTER OSCILLATOR:

Refer to Dwg. No. 0137-C-SD. This drawing shows schematics of circuits located on board 8. The 10KC master oscillator schematic is shown in the upper left hand corner of the drawing. Transistors Q801 and Q802 with the associated cross coupling networks form a relaxation oscillator. The collectors drive the center-taped primary winding of coupling transformer T801. The secondary of this transformer drives the charge pump. This circuit is quite conventional

and therefore will not be discussed in detail. The output to drive the counter is taken at the cathode end of diode D803. At this point the waveform is only positive going at the end of each oscillator cycle, so that the counter is always triggered at the time when the millivolt step at the output of integrator is being generated. This point swings from approximately +8 to +12 volts. Terminal 5 marked "OSC" connects this signal to the counter.

The oscillator is gated on and off by two transistor switches, Q803 and Q804 driven by signal M arriving at terminal 6. The RC network consisting of R806 and C805 delay the gating signal M, so that when it goes negative Q804 turns off first, unclamping the base of Q802, before the base of Q801 is unclamped. This forces the oscillator to start always with the same phase.

OSCILLATOR GATE

The gating signal M is generated on the comparator board No. 6 as an output of the "AND" gate consisting of diodes D613, D614 and D609 which are shown in Dwg. No. 0136-C-SD. Inputs to all three diodes must be negative to start the oscillator. The timer T goes negative at the very beginning of conversion period. The comparator output K goes negative when the proper one of F4 or G4 relay contact is closed as already mentioned in the"DESCRIPTION OF CIRCUIT FUNCTIONS." What actually turns the oscillator on is the negative going collector of Q607 driven by a delayed E3 coil driving signal. The time delay set by C609 and the associated resistors in the base of Q607 allows all relay switching transients to decay before the oscillator (and thus the ramp) is started. The timing chart, Figure 4, shows this gating waveform. The oscillator is normally stopped by the positive going comparator output. However, during the up-ranging time when the comparator does not go positive within the conversion period, the master timer output T stops the oscillator.

SYNCHRONOUS RAMP GENERATOR:

The SYNCHRONOUS RAMP GENERATOR comprises two basic circuits. The charge

pump and the integrator. Both circuits are located on board No. 8 and are shown schematically in the lower half of Dwg. No. 0137-C-SD. Transistors Q809 and Q810 together with the secondary winding of transformer T801 form the "charge pump" circuit. Transformer T801 is driven by the master oscillator as already explained. The secondary output is essentially a square wave, 3 volt peak-to-peak amplitude and with a period of approximately 100 microseconds. To obtain a low offset voltage the transistors in this circuit are driven at the base-to-collector junctions. The driving current is limited by resistor R818. During the negative half cycle, that is when terminal 5 of the secondary winding is negative with respect to terminal 4, Q809 will be "on" and Q810 will be "off." Under this condition the source capacitor, C809, will charge to -9.3 volts,since the emitter of Q809 is connected through R839 to terminal 16 which is at that potential. During the other half cycle, or when terminal 5 of the transformer secondary becomes positive, Q809 is "off" and Q810 is "on." The emitter of Q810 is connected to the integrator input which is at ground potential. The charge stored in C809 will now flow into the integrator input causing its output to rise by 1 millivolt. This quantitized charge flow repeats with each cycle of the oscillator, generating a staircase at the integrator output. The name "synchronous ramp generator" is derived from the fact that the steps of this ramp are generated synchronously with the oscillator frequency.

The integrator amplifier is a conventional circuit with two differential and one single ended stage all direct coupled. It is stabilized before each conversion period by a negative feedback loop switched in and out by a pair of relay contacts marked $E_3R$ on terminals 10 and 11. Potentiometer R824 is used to adjust the base current to the input transistor Q811. The base current here is approximately 0.5 microamp. The adjusting of zero reference level is done by means of a potentiometer mounted on the mother board and adjustable through an opening in the front panel. This potentiometer is wired to points

P1, P3 and P2 (connectors 18, 19 and 20 respectively). Point P2 is the wiper which returns to the minus fifteen volt supply through R835. The other two points, P1 and P3 are connected to the emitters of the differential input transistors. The ramp output is taken from the wiper of the potentiometer connected between points P5 and P6 (terminals 22 and 23) also mounted on the mother board and accessible through the front panel. This control is marked "CALIBRATE". The actual ramp signal, called "R", is wired to connector 24.

For good stability with temperature both the charge source capacitor C809 and the two integrator capacitors C810 and C811 are hermetically sealed polystyrene types.

The amplifier bandwidth ranges from DC to over 50 KC. The voltage gain is approximately 3500. The ramp at the collector of Q815 goes from zero to approximately 20 volts. It is attenuated to zero to one volt by means of resistors R819, R820 and R821.

POLARITY LOGIC

The polarity logic circuit is located on board 7. It is shown schematically in Dwg. No. 0135-C-SD. The polarity reversing Flip-Flop is shown in the upper right hand corner of the drawing. The circuit itself is conventional and will not be discussed. The switching functions of the logic gates, however, will be explained in some detail. The polarity reversing relays F2, G2 and F4 and G4 are shown in the block diagram Dwg. No. 0188-B-SD. The polarity reversing Flip-Flop actuates only the F2 and G2 relays. Another circuit functionally dependent on the states of F2 and G2 located on the attenuator board actuates the F4 and G4 relays.

The collector of Q706 wired to terminal 5 drives the F2 coil and the collector of Q708 wired to terminal 15 drives the G2 coil. The bases of both are driven by TRL logic circuits. Q706 is driven by Q705 with a two resistor "AND" gate at its base (R705 and R706). Q708 is driven by Q707 and two resistor "AND"

gate (R707 and R708). The "AND" gate inputs are the two outputs of the polarity reversing Flip-Flop and the delayed and inverted master timer complement T' appearing at the collector of Q720. The T' signal is delayed for approximately 2 milliseconds by capacitor C717 and the associated resistive network at the base of Q720. This delay time slows down switching of F2 or G2, so that the E1 contacts open first and disconnect the sampling capacitor from the attenuator output.

Q701 and Q704 are Nixie drivers whose collectors are wired to terminals 16 and 17 and are labelled "+" and "-" respectively. A plus or minus sign is displayed depending on the state of the polarity reversing Flip-Flop. The switching functions for G2 and F2 relays may be written as follows:

$$G2 = (+)\ Tc$$

$$F2 = (-)\ Tc$$

Where Tc is the delayed and inverted pulse of T' at the collector of Q720. A trigger pulse applied between capacitors C701 and C702 of the polarity reversing Flip-Flop will change its state, which will cause a change in the polarity display as well as reversing the states of F and G coils.

The polarity trigger pulse is generated by a circuit shown in the upper right hand corner of the schematic. Coil driving signals F4 and G4, arriving at terminals 11 and 14, feed the "OR" gate consisting of diodes D704 and D705. The resulting negative going pulse of the gate output, which occurs when the sampling capacitor is switched over to the comparator input, is coupled to the base of Q709 through resistor R739. Capacitor C716 delays the turn on of Q709 approximately ½ millisecond, so that the comparator output reaches its saturated level of -10 volts or + 5 volts depending whether the sampling capacitor is switched over with the right or wrong polarity. The positive going pulse at the collector of Q709 is differentiated by capacitor C719 and coupled to an in-

hibitor circuit employing Q710 and Q711. In what follows, this pulse will be referred to as the polarity trigger pulse. The inhibitor circuit operates as follows. The comparator output arriving at terminal 12 (marked "K") is coupled to the base of Q711. When it is negative, which signifies the right polarity for conversion, Q711 will be turned on and Q710 will be off because its base is set at approximately + 3 volts by resistive divider R719 and R720. Under this condition the polarity trigger pulse is clamped to minus ten volts by the emitter of Q711. The polarity reversing Flip-Flop will not be triggered and thus all circuits of the polarity reversing logic will remain in their original state. With the wrong polarity of the sampling capacitor however, Q710 will have its base-to-emitter junction forward biased as soon as the comparator output rises above + 3 volts. The small bias current supplied by the emitter resistor R722 causes the collector of Q710 to establish a quiescent level of approximately -13.5 volts. The polarity trigger pulse will now pass to the collector of Q710 and the polarity reversing Flip-Flop will be triggered. The states of the F and G relays will be reversed and the polarity sign will change. The various pulse waveforms mentioned in the above discussion are shown in the timing chart Figure 4.

The simplified switching function of the polarity reversing signal may be written as follows:

$$P_S = P_T K$$

where $P_S$ is the pulse at the trigger input of the polarity reversing Flip-Flop, $P_T$ is the polarity trigger pulse generated at the collector of Q709 and differentiated by C719, and K is the comparator output.

RELAY SEQUENCE PROGRAMMER

This circuit is shown in block form on Dwg. No. 0188-B-SD. It generates switching functions E1, F2, G2, E3, F4 and G4. In reality it consists of several

separate circuits distributed throughout the entire voltmeter. For convenience of interwiring, the circuits are usually placed on boards where the proper input signals are available or where their outputs are used to switch relay coils. The F2 and G2 switching functions were already encountered in the discussion of polarity logic and will not be repeated here.

The switching signal of the E1 relay coil is produced by a circuit located on the comparator board, No. 6, and is shown in schematic diagram 0136-C-SD. Signal E1 which appears at the collector of Q605 is wired to terminal 18. The base of Q605 is coupled via resistor R626 to the output of a three diode "AND" gate employing diodes D610, D611 and D612. One diode, D610, leads to the master timer output "$T_1$" at terminal 8. The other two have their cathodes on two RC networks employed here to delay the switching pulses so that a proper time relation is maintained between the E1 and E3 signals. The E3 signal, generated at the collector of Q606 and connected to terminal 17, lags E1 when the transistors are being turned off. The turn on of both transistors Q605 and Q606, however, occurs at approximately the same time. The following sequence of events is responsible for this time relationship.

When T goes negative (approximately 4 volts) Q605 (E1) turns off immediately because its base follows the master time T. Q606 (E3), however, because of its base being connected to C608 will turn off approximately 5 milliseconds later, or the time required for C608 to discharge to ground level. When at the end of the conversion cycle T goes positive again, the turn on time of Q605 and Q606 will be determined by the combined time constant of their base circuits.

The two transistors driving F4 and G4 relay coils and the associated logic gates are located on the attenuator board, No. 9, and shown at the bottom of schematic diagram No. 0140-C-SD. Q901 operates the F4 and Q902 operates the G4 coil. Both transistor bases are driven by "AND" gates whose outputs depend on the state of the F2 and G2 relays as well as on the inhibit signal derived from the E3 switching function which is delayed slightly by R918 and C903 to make sure that E3 contacts open before either F4 or G4 are closed. F4 will close only when F2 is closed because then the diode, D914, whose cathode is connected to G2 will unclamp the base of Q901. G2 is the complement of F2 and therefore it is positive when F2 is at ground which is the "ON" state of the relay. A similar argument holds for Q902 driving G4. The master timer complement T' at terminal 7 is coupled to both bases via diodes D915 and D917. The purpose of these two diodes is to turn off both F4 and G4 relays without delay when T' goes negative at the end of conversion period.

UP-RANGING AND DOWN-RANGING GATES

The two circuits which generate the up-ranging and the down-ranging signal for the attenuator programmer are both located on the comparator board, No. 6, and are shown schematically in the upper half of drawing No. 0136-C-SD.

The output of the number 9 Nixie driver of the first digit is connected to terminal 5. This signal is coupled to the base of Q601 via diode D602 and a resistive divider to set the base potential of Q601 below ground when 9 is on, (at + 5 volts) so that Q601 is cut off. When 9 turns off going more positive, Q601 turns on. C601 and R605 differentiate the inverted 9 signal which then is applied to one input of an "AND" gate consisting of diodes D605 and D604. Master timer pulse T, delayed by R609 and C602 is applied to the other input. This signal inhibits the output of this gate while the counter is being reset. The gate output is coupled via diode D606 to the base of Q602 which is employed together with Q603

in a conventional monostable multivibrator circuit. The multivibrator period is set by R608 and C603 to be approximately 150m sec. Why this was done will be explained when the down-ranging gate is discussed. The collector of Q602 swings from ground up to +8 volts every time number 9 of the most significant digit goes off, except during the reset of the counter. This signal wired to terminal 7 and labelled "X" is used as an up-ranging command for the attenuator programmer.

A zero in the most significant digit at the end of a conversion is used to generate the down-ranging signal. The zero Nixie driver output applied to terminal 10 couples via diode D603 to a network which delays it somewhat and sets a proper on and off level at one input to the two diode gate employing D607 and D608. Master timer complement T' differentiated, is applied to the other input. Capacitor C605 delays the zero signal by approximately 1m sec., so that the gate has no output during the reset transient. The gate output will turn off Q604 for the period set by R617 and C606, which is approximately 1m sec., when T' is negative going if at that time the most significant digit is in the zero state. This down-ranging pulse is, however, inhibited by clamping the collector of Q604 through diode D601 to the complement of the up-ranging pulse at the collector of Q603, so that the attenuator programmer does not receive the down-ranging command immediately following the up-ranging cycle in cases when the counter may have a zero in the most significant digit due to an over-count of less than 100 counts. To generate this inhibiting signal it was necessary to use a monostable multivibrator in the up-ranging circuit in order to extend it in time to where the down-ranging pulse occurs. The down-ranging pulse is brought out to terminal 6 (labelled Y). Its amplitude is + 8 volts and its duration approximately 1 millisecond. Both X and Y waveforms are shown in the timing chart Figure 4.

ATTENUATOR PROGRAMMER:

The attenuator programmer consist of two gated flip-flops and a TRL decoding matrix. The two gated flip-flops are located on the programmer logic board, No. 7, and are shown schematically in Dwg. No. 0135-C-SD. This circuit has two inputs, X and Y, (the up-ranging and the down-ranging signals) and four outputs 1, 1', 2 and 2', which feed the decoding matrix located on comparator board, No. 6, and shown in schematic diagram No. 0136-C-SD. The matrix outputs A, B, C, D, and D' drive the attenuator ranging relays.

The purpose of this whole circuit is sequential switching of the A, B, C, D and D' relays, maintaining a forward sequence, that is from A to B to C to D every time the down-ranging pulse Y is applied, and reversing the sequence to switch from D to C to B to A every time the up-ranging pulse X is applied. It may be helpful to first examine the input-output conditions of this circuit in terms of switching algebra equations. For the outputs we can write:

$$A = 1'2$$

$$B = 12'$$

$$C = 1'2'$$

$$D = 12$$

The outputs are considered to be in the "on" state when at ground level, but the 1 and 2 switching functions are "on" when positive.

Notice that in order for the outputs to follow a forward sequence (A-B-C-D) the second flip-flop whose outputs are 2 and 2', must change state every time output 1 of the first flip-flop goes positive.

The same observation reveals that for the D-C-B-A sequence the second flip-flop must change states when output 1' of the first one goes positive.

Thus the direction of the switching sequence depends on which output of the first flip-flop is triggering the second one. That is to say, the two stage binary counter thus formed will count in either the forward or the reverse dir-

ection depending on whether the Y or the X pulse triggers it. The trigger function T1 for the first stage is given by:

$$T1 = (X + Y)$$

which holds true for both directions.

The trigger function for the second stage, T2F, to result in a forward sequence is:

$$T2F = Y1$$

and for the reverse sequence the T2R trigger function is given by:

$$T2R = X1'$$

The trigger input to the second stage T2 consisting of the two functions combined is given by:

$$T2 = Y1 + X1'$$

Referring now to schematic drawing 0135-C-SD we can recognize the circuits performing the switching functions discussed above. The Y and X signals come in on terminals 7 and 8. They are coupled via resistors R709 and R710 to a transistor "OR" gate consisting of Q712, Q713, Q714 and Q715, which generates the trigger function T1 for the first flip-flop. Another transistor "OR" gate consisting of Q716, Q717, Q718 and Q719 triggers the second flip-flop. Inputs to this "OR" gate employ two resistor "AND" gates, one of which provides the Y1 input using resistors R740, R743 and R744, and the other provides the X1' input via resistors R741, R742 and R745. The X and Y pulses arrive at the gate inputs slightly delayed due to capacitors C713 and C714 so that the first stage established its new state before the second is triggered.

The flip-flops employing transistors Q721, Q722, Q723 and Q724 are completely conventional and will not be discussed here. Their inputs are wired to terminals 24, 25, 26 and 27 which feed the decoding matrix located on board No. 6. A word of explanation about the function of diode D707. This diode

clamps the down-ranging signal Y to the D output of the matrix (at terminal 20) which is on ground when the attenuator is in its lowest range. This locks out the down-ranging cycle permitting measurements of potential below 100 millivolt levels.

The decoding matrix is shown schematically in drawing number 0136-C-SD. It consists of four conventional transistor-resistor logic gates and an inverter for D'. The voltage levels of inputs 1, 1', 2 and 2' are + 8 volts when "on" and approximately -11 volts when "off". Transistors Q610, Q611, Q612 and Q613 marked A, B, C, and D have their collectors brought out to terminals 22, 21, 20 and 19. The D' collector is on terminal 23. Each output transistor has a 0.1 uf capacitor at its base, which prevents it from turning on during switching transients.

The lowest range of the attenuator calls for A to be "on" when D' is "off". A diode switch employing D619 and D620 between the D' collector and the base of "A"provides this switching logic.

ATTENUATOR AND MEMORY CIRCUITS

Schematic diagram No. 0140-C-SD shows the attenuator and memory circuit which are located on board (No. 9). The attenuator consists of 12 precision wire wound resistors. Nine 1 meg. resistors connected in series are represented schematically as R901 - 909. The other three are R910, R911 and R912. Terminal 27 marked ATH, is the "HIGH" input. It is connected to R901 - 909. The "LOW" input (terminal 25 marked ATL), is connected to R912 through contacts of relay D'. The two terminal output of the attenuator is coupled via series resistors R916 and R917 to two E1 contacts S913 and S912 which connect the memory capacitor to the attenuator output. The input to output ratios, depending on which relay contacts are closed, are tabulated on the next page:

| Contacts Closed | Attenuation Ratio |
|---|---|
| A, D' | 1000:1 |
| B, D' | 100:1 |
| C, D' | 10:1 |
| A, D | 1:1 |

Resistors R914 and R915, connected in series with relay contacts leading to a common output point as well as resistor R913, make the attenuator output resistance approximately 1 Megohm for all ranges, so that the sampling circuit time constant does not depend on the attenuation ratio.

The common point of contacts A, B and C (one of the attenuator outputs) is connected to terminal 24 marked ATC. For zero check this point is grounded by the selector switch contacts. Terminal 26, marked ATB, is wired to the attenuator point where the ratio is 100:1. The selector switch applies a negative calibration voltage of approximately -9 volts to this point when set in "CALIBRATE" position. This is why the calibrate voltage as seen on the display appears to be in the order of -900 volts. For the same reason, when the selector switch is changed from ZERO to CALIBRATE position without stopping in HOLD until the decimal point stops advancing, the decimal point may not advance to its extreme position on the right but hang up in the range where the input voltage and the calibration voltage establish a level of less than 1 volt at the attenuator output.

Three neon lights connected across various points on the attenuator limit the voltage across relay contacts as well as on the sampling capacitor to approximately 75 volts in the case when high input voltage is applied and the attenuator has its low range switches in. The low range switch D is rated for one thousand volts operating potential.

Relays F2, G2, F4 and G4 connect the sampling capacitor C901 between terminal 10, marked E3G, which is the comparator input and terminal 17, marked R,

which is the ramp output. Polarity reversal is accomplished by closing either F2 and F4 contacts or G2 and G4 contacts. When the "HIGH" input terminal is positive with respect to the "LOW" input terminal the G2 and G4 contacts are closed. Reversing the input polarity will cause the G2 and G4 relay to open F2 and F4 to close.

The third contact pair of relay E1 S911 stabilizes the comparator amplifier. E3 relay has two pairs of contacts one of which is used to stabilize the integrator amplifier and the other which grounds the comparator input during its stabilization period. Capacitor C902 functions as a low pass filter at the ramp output.

Input and output signals as well as all switching functions are identified by symbols and connector numbers at the left of the schematic drawing. All of these as well as the Q901 and Q902 circuits were encountered in previous discussions.

To suppress inductive voltage transients during turn-off each relay coil is shunted by a silicon junction diode.

MASTER TIMER

The master timer is located on board No.8. Its schematic is shown in the upper right hand corner of drawing No. 0137-C-SD. It is a conventional astable multivibrator with emitter follower outputs. The output waveforms are shown in the timing chart, Figure 4. The "T" output taken at the emitter of Q806 is at -4 volts for approximately 0.15 second and switches to a level of +7 volts for approximately 0.85 seconds. Its negative level marks the conversion period and the positive level marks the readout period. The output at the emitter of Q807 is the complement of T.

Transistor Q816 whose base is connected via R838 to terminal 7 (marked I) shunts the base of Q805 thus locking the master timer in the readout state, when I and T are connected together. This switching is accomplished by an externally programmed relay contact closure when operation with "read on command" is desired

as described in the OPERATING INSTRUCTIONS.

THE SELECTOR SWITCH

The mother board wiring diagram Dwg. No. 0386-B-SD shows the wiring of selector switch contacts. The following explanation may be helpful however to understand what the switch does in any of the five positions.

OFF:
1) Transformer primary disconnected from power line.
2) GUARD connected to signal ground.

AUTO:
1) Transformer primary connected to power line. (all positions except "OFF").
2) GUARD connected to signal ground.

ZERO:
1) GUARD terminal open.
2) Attenuator output (ATC) connected to signal ground.
3) Attenuator "LOW" input connected to signal ground.

HOLD:
1) GUARD terminal connected to signal ground.
2) Collector of Q604 connected to signal ground to inhibit the down-ranging signal "Y"
3) Connections made in ZERO position open.

CAL:
1) GUARD terminal open.
2) Calibration voltage applied to attenuator point ATB.
3) Attenuator "LOW" input connected to signal ground.
4) Connections made in "HOLD" position open.

## V. ADJUSTMENTS AND CALIBRATION

There are a total of three adjustments and one calibration control in the instrument. Each adjustment and calibration employs a fifteen turn screwdriver adjust potentiometer. The ZERO and CALIBRATE controls are accessible through the front panel. The other two adjustments, one for voltage supply (setting the -15 volt level), and the other to set the bias current for the integrator input transistor are located on printed circuit boards inside the instrument.

### ZERO ADJUSTMENT

Turn the instrument on and allow it to warm up. With the selector switch in the "ZERO" position turn the "ZERO" control potentiometer clockwise until the least significant digit displays the number "one", as a steady repetitive reading. Under this condition the sign, either positive or negative, will remain unchanged. Now turn the "ZERO" control potentiometer slowly counter clockwise, at the rate of approximately 1/4 turn per second, and stop at the point where the sign will start to alternate between positive and negative. From this point make one more counter clockwise turn to arrive at the correct "ZERO" setting.

### CALIBRATION

The calibration number appears in the lower left hand corner (below the polarity indicator) of the readout window. With the instrument warmed up, set the selector switch to "CAL" position and observe the readout. The decimal point should be in the extreme right hand position and a minus

sign should be displayed. The number appearing on the readout should be the same as that appearing on the window. If this is not true, adjust the "CAL" control to obtain the correct reading.

While calibrating the instrument the probe terminals may be left connected across a DC potential of any level up to 999 volts and no error in calibration will result.

INTEGRATOR AMPLIFIER INPUT BALANCE

The bias current for the integrator input stage is adjustable by a potentiometer located on the ramp generator board No. 8. To make this adjustment an oscilloscope having a sensitivity of at least 10MV/CM is necessary.

Unplug the instrument and take the cover off, by taking out the four screws at the rear. This will allow the cover to slide back. Locate board No. 8 and remove it. Using schematic diagram No. 0137-C-SD locate master timer output "T". It is on connector No. 8 counting from left to right facing the board. Also locate connector No. 11 which is the integrator output. Solder approximately 12 inches of insulated wire to connector 8 and connector 11. Replace the board making sure that nothing is shorted by the soldered leads. Turn the instrument on and connect the oscilloscope ground to the "GUARD" terminal. Trigger the oscilloscope externally on the leading edge of the negative going pulse T. Set the selector switch in ZERO position and connect the oscilloscope probe to the integrator output. Observe the slope of the integrator output during the 0.15 second negative excursion of master timer output "T".

Vary the potentiometer on top of board to obtain a positive slope of approximately 15 millivolts per 100 milliseconds, which indicates a correct input bias level. Unplug the power cord, unsolder the two temporary connections and re-assemble the cover.

POWER SUPPLY ADJUSTMENT

Because of the 10 percent variation in the nominal break-down voltage of the reference zener diode used, an adjustment is provided to set the -15 volt line to its nominal value. The potentiometer for this adjustment is located on power supply (board No. 5). This potentiometer when set at the factory, (after installation of a reference zener diode) should stay set without readjustment, unless the reference zener diode for which it was set is replaced.

When for any reason adjustment is necessary refer to power supply schematic Dwg. No. 0138-C-SD. The -15 volt line is the first connector on the left. Measure this voltage with respect to GUARD and adjust the potentiometer to set it within $\pm$ 1 percent of -15 volts.

NOTE: This instrument may be used to measure its own internal supply potentials which are all with respect to GUARD. The GUARD and LOW terminals of the probe should be connected together and the HIGH terminal used to probe the supply potentials.

## VI. WARRANTY

Princeton Applied Research Corporation warrants each instrument of its own manufacture to be free from defects in material and workmanship. Obligations under this Warranty are limited to replacing, repairing or giving credit for the purchase price, at our option, of any instrument returned PREPAID to our factory for that purpose within ONE YEAR of delivery to the original purchaser. Instruments returned to the factory are accepted only when prior authorization has been given by an authorized representative of Princeton Applied Research Corporation.

This Warranty shall not apply to any instrument, which our inspection shall disclose to our satisfaction, to have become defective or unworkable due to abuse, mishandling, misuse, accident, alteration, negligence, improper installation, or other causes beyond our control. (Tubes, choppers, and lamp bulbs are exempted from this Warranty.)

Princeton Applied Research Corporation reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This Warranty is in lieu of, and excludes all other warranties or representations, expressed, implied or statutory, and all other obligations or liabilities of Princeton Applied Research Corporation including special or consequential damages, and no other source is authorized to assume for Princeton Applied Research Corporation any other liability.

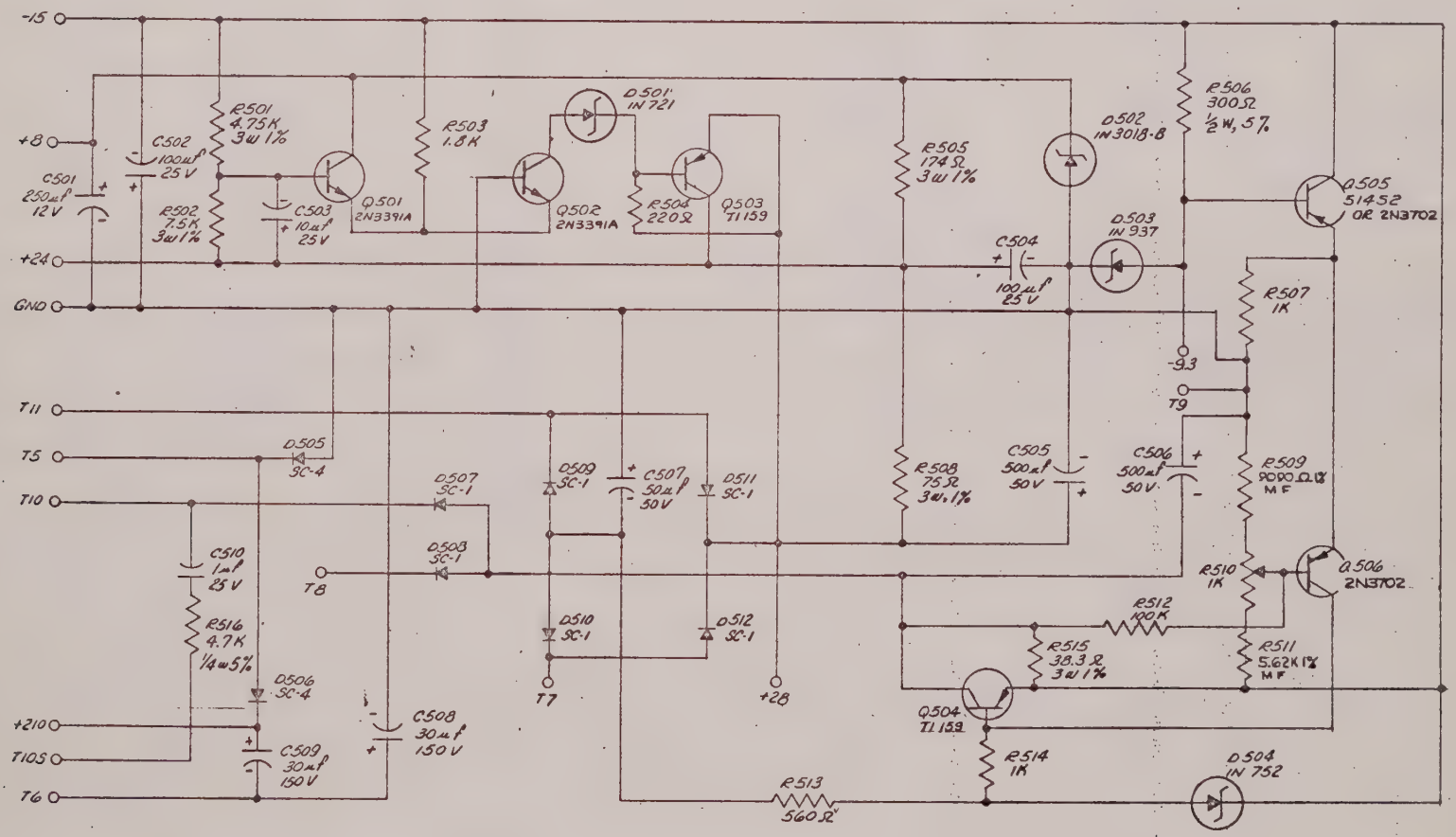
Princeton Applied Research Corporation
Princeton, New Jersey

# TRANSISTOR SUBSTITUTIONS

Because of recent difficulties experienced in procuring 2N3391A type transistors, it has been necessary to substitute other types for the 2N3391A in some units of the PAR CS-3.1 Digital Voltmeter. As the substitute transistors are the equivalent of the 2N3391A in each application, instrument performance is in no way degraded.

Whether the instrument is shipped with the 2N3391A type transistor, or with the substitutes, the schematics specify the 2N3391A. The following list of the affected transistors and the substitute in each case is provided to prevent any possible confusion which might result from the inconsistancy between the transistor type called for in the schematics and the types actually used in the instrument.

| Transistor "Q" Number | Type | Replace With |
|---|---|---|
| 801 | 2N3391A | 2N3566 |
| 802 | " | " |
| 805 | " | " |
| 808 | " | " |
| 816 | " | " |
| 811 | " | 2N3711 |
| 812 | " | " |
| 813 | " | " |
| 814 | " | " |
| 501 | " | " |
| 502 | " | " |




| 1 / -15 | 2 / +8 | 3 / +24 | 4 / GND | 10 / -9.3 | 19 / T9 | 20 / T5 | 21 / T10 | 22 / T8 | 23 / T7 | 24 / +210 | 25 / T11 | 26 / +28 | 27 / T6 | 12 / T10S |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

NOTE:
ALL RESISTORS ARE ½ w 10% UNLESS OTHERWISE NOTED

MODEL CS 3.1

POWER SUPPLY SCHEMATIC

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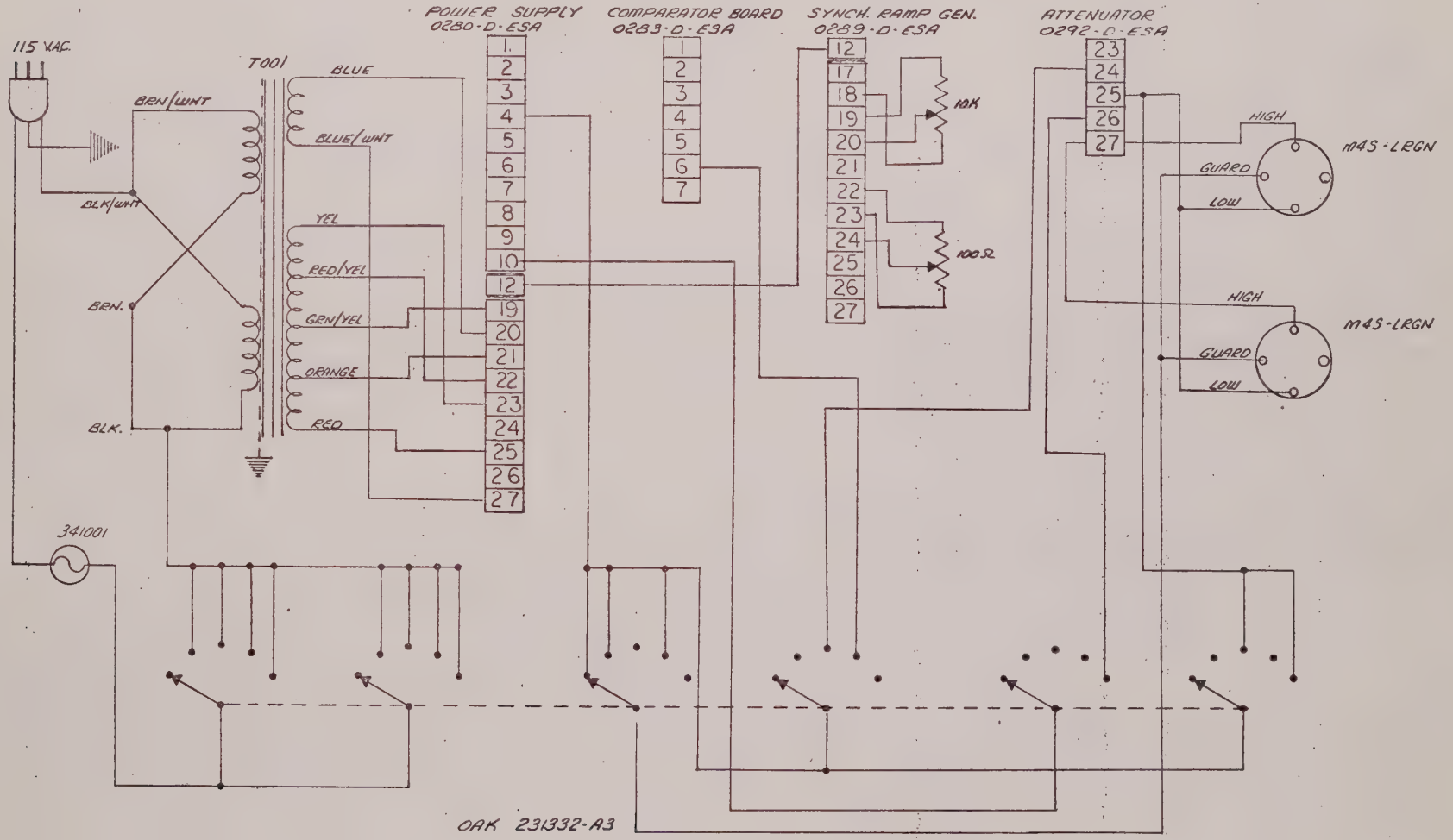
CIRCUIT BOARD NR PS 0280

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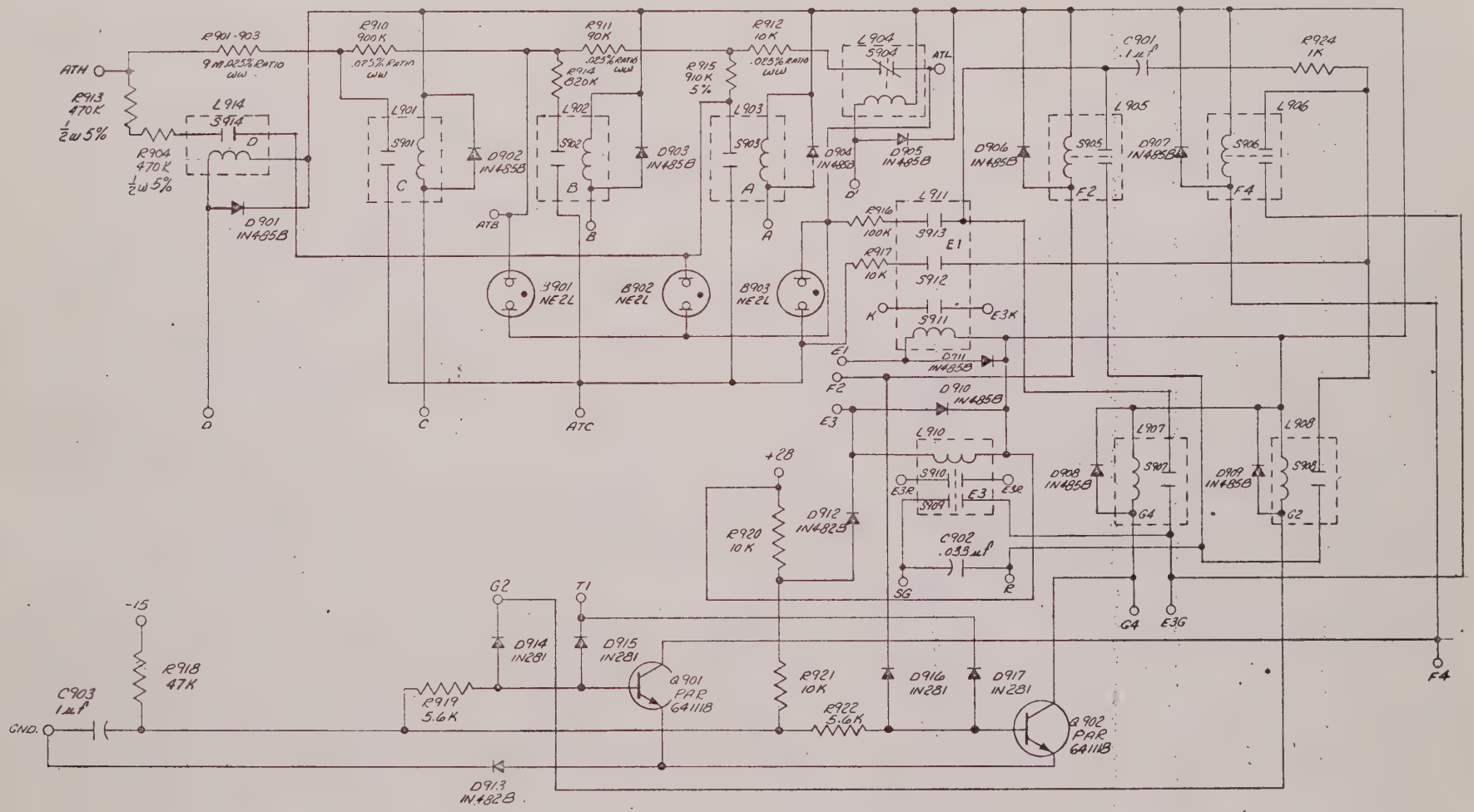
MODEL CS-3.1

MOTHER BOARD - WIRING SCHEMATIC

CIRCUIT BOARD No. MB0295




| 1 -15 | 2 NC | 3 GRD | 4 F2 | 5 E3R | 6 E3R | 7 T1 | 8 SG | 9 E3K | 10 E3G | 11 F4 | 12 K | 13 E1 | 14 G4 | 15 G2 | 16 E3 | 17 R | 18 D | 19 C | 20 B | 21 A | 22 D' | 23 +28 | 24 ATC | 25 ATL | 26 ATC | 27 ATH |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

NOTE: ALL RESISTORS ± W, 10% UNLESS NOTED.

PIN CONNECTIONS

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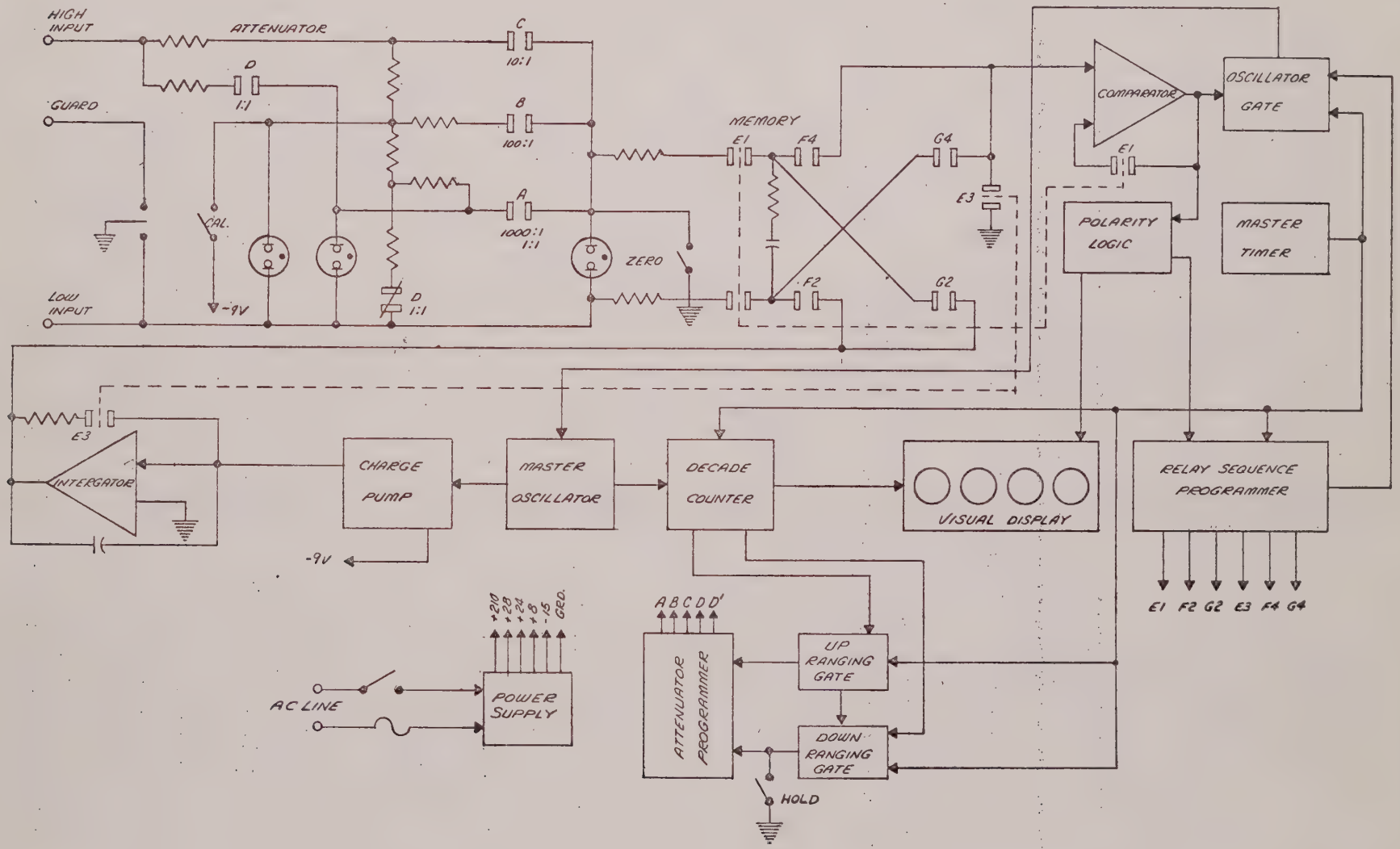
MODEL CS-3.1

ATTENUATOR

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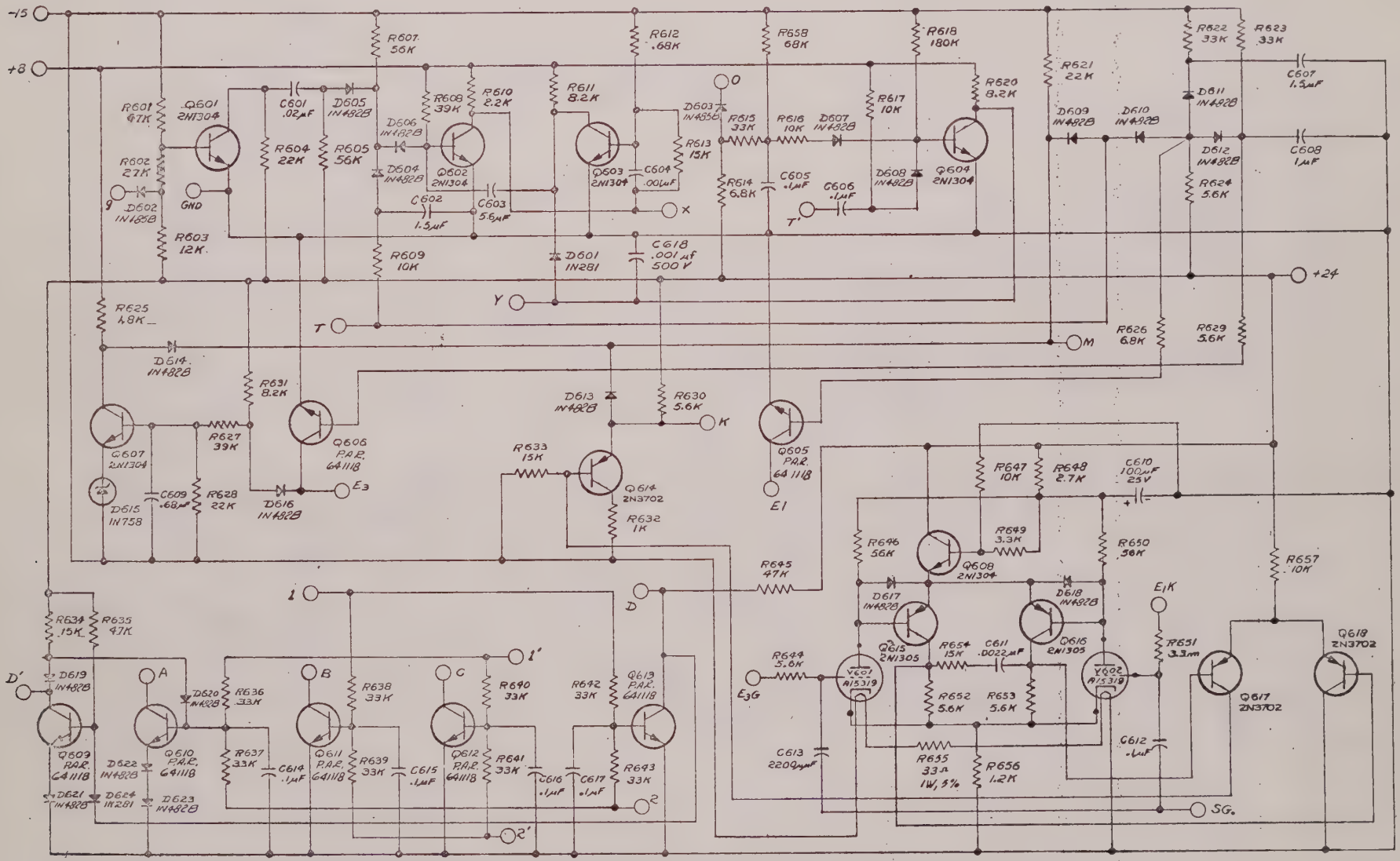
MODEL CS 3.1 DIGITAL VOLTMETER




NOTE: ALL RESISTORS ¼ W 10% UNLESS OTHERWISE NOTED

PIN CONNECTIONS

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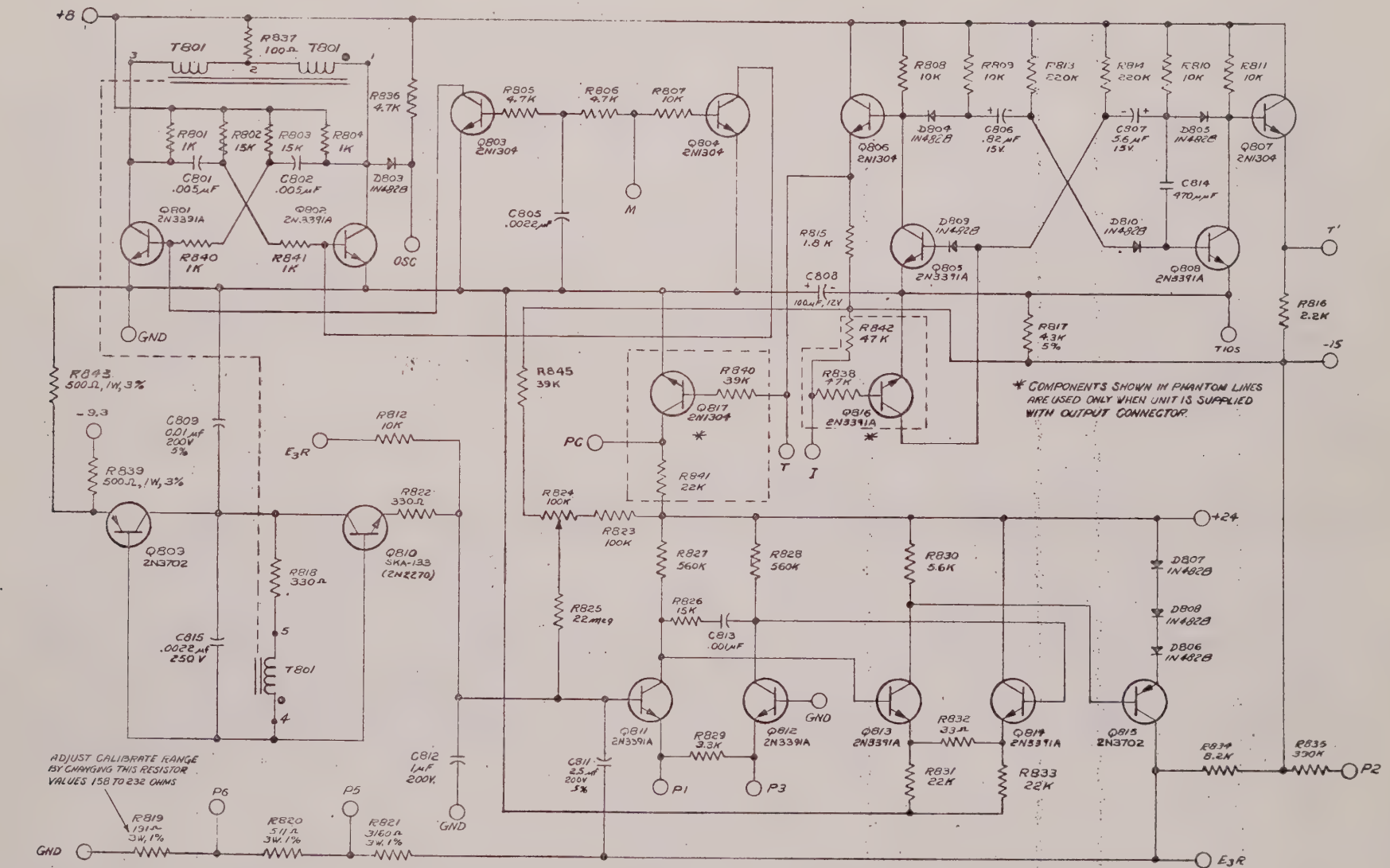
MODEL CS 3.1

COMPARATOR




* COMPONENTS SHOWN IN PHANTOM LINES ARE USED ONLY WHEN UNIT IS SUPPLIED WITH OUTPUT CONNECTOR.

| 1 -15 | 2 +8 | 3 +24 | 4 GND | 5 OSC | 6 M | 7 I | 8 T | 9 T' | 10 E3R | 11 E3R | 16 -9.3 | 18 P1 | 19 P3 | 20 P2 | 22 P5 | 23 P6 | 24 R | 12 T10S | 21 PG |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

PIN CONNECTIONS

NOTE ALL RESISTORS ¼ W, 10% UNLESS OTHERWISE NOTED

MODEL CS3.1

SYNCHRONOUS RAMP GENERATOR

CIRCUIT BOARD NO. PC-C282

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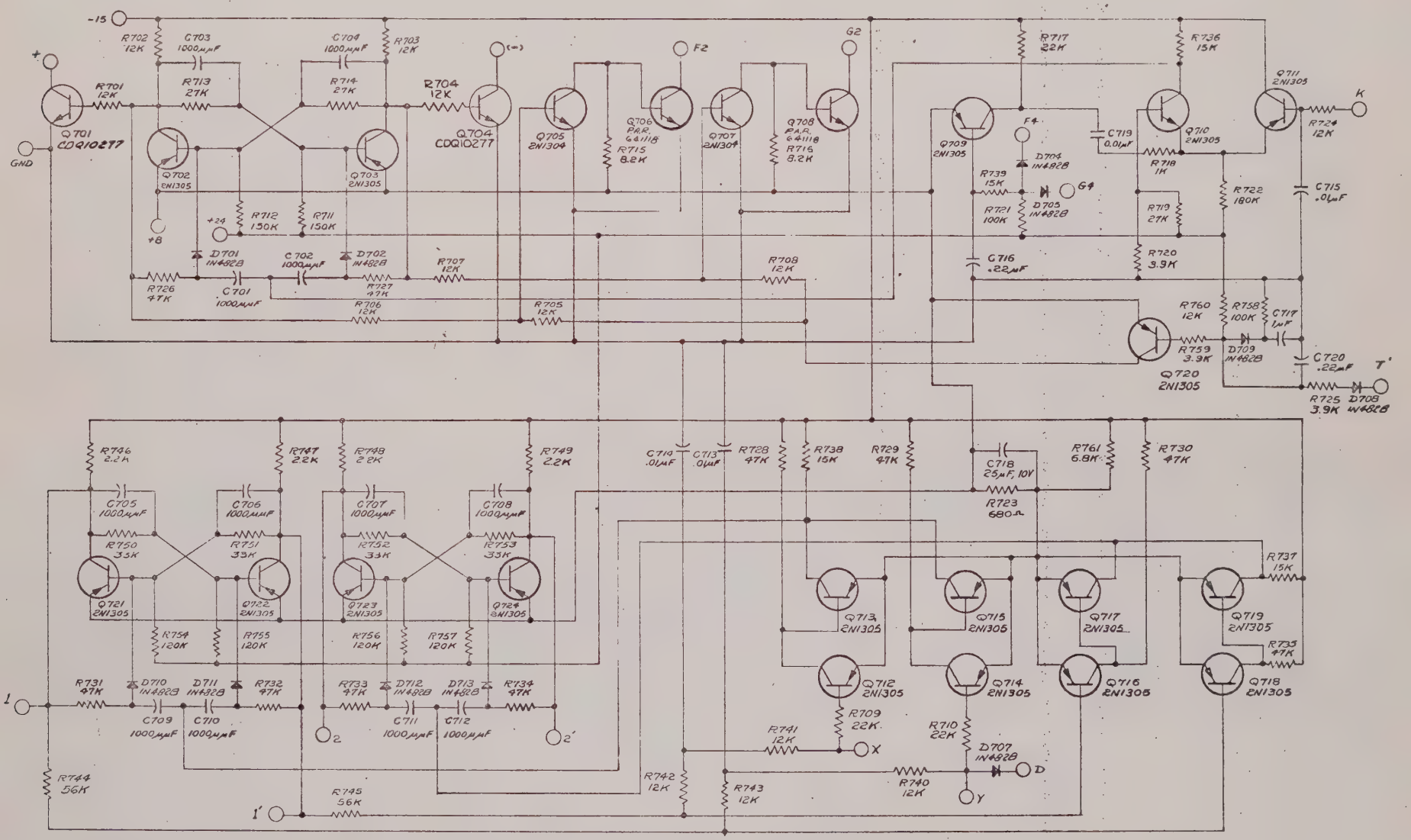


| 1 -15 | 2 +8 | 3 +24 | 4 GND | 5 F2 | 6 NC | 7 Y | 8 X | 9 NC | 10 T' | 11 F4 | 12 K | 13 NC | 14 G4 | 15 G2 | 16 + | 17 (-) | 18 NC | 19 NC | 20 D | 21 NC | 22 NC | 23 NC | 24 1' | 25 1 | 26 2 | 27 2' |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

PIN CONNECTIONS

NOTE: ALL RESISTORS 1/4 W, 10% UNLESS NOTED.

MODEL CS 3,1

PROGRAMMER LOGIC

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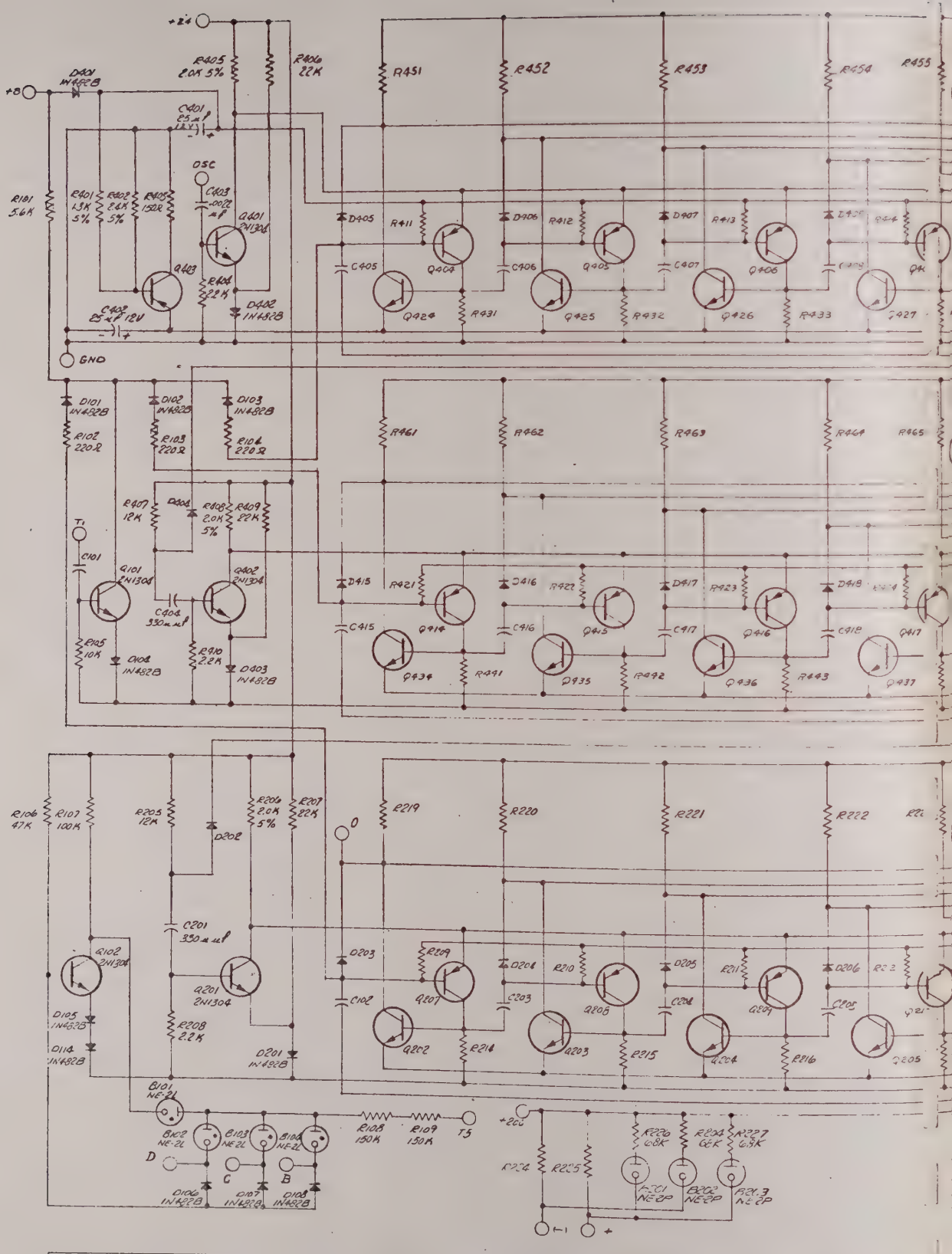
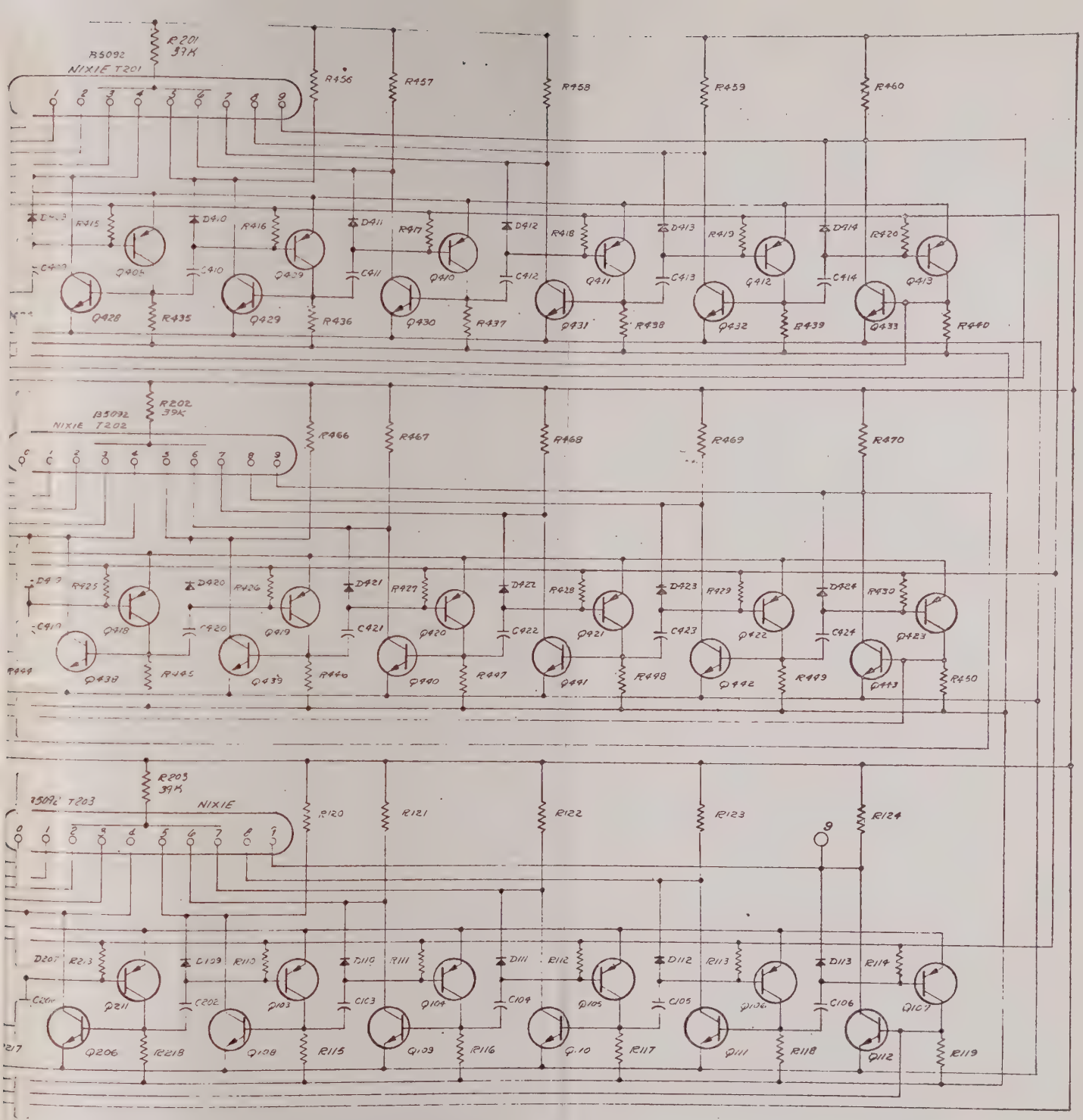



MODEL CS-3.1

COUNTER

CIRCUIT BOARD No 1
CIRCUIT BOARD No 2
CIRCUIT BOARD No 3




| TABLE OF COMPONENT VALUES | |
|---|---|
| R451 TO R459 | 1meg |
| R461 TO R469 | |
| R219 TO R225 | |
| R120 TO R124 | |
| R411 TO R430 | 1K, 10% |
| R209 TO R213 | |
| R110 TO R114 | |
| R431 TO R450 | 1K, 5% |
| R214 TO R218 | |
| R115 TO R119 | |
| ALL DIODES IN4458 EXCEPT AS MARKED | |
| ALL CAPACITORS ARE .01 50V EXCEPT AS MARKED | |
| ALL PNP TRANSISTORS ARE 2N1305 EXCEPT AS MARKED | |
| ALL NPN TRANSISTORS ARE RAYTHEON EXCEPT AS MARKED | |
| ALL RESISTORS ARE ¼ W 10% UNLESS OTHERWISE NOTED | |
| R460, R470 220H ¼ W. 10% (ECW71) | |

NOTE: THE FIRST DIGIT OF EACH COMPONENT NUMBER INDICATES THE BOARD ON WHICH THE COMPONENT IS LOCATED

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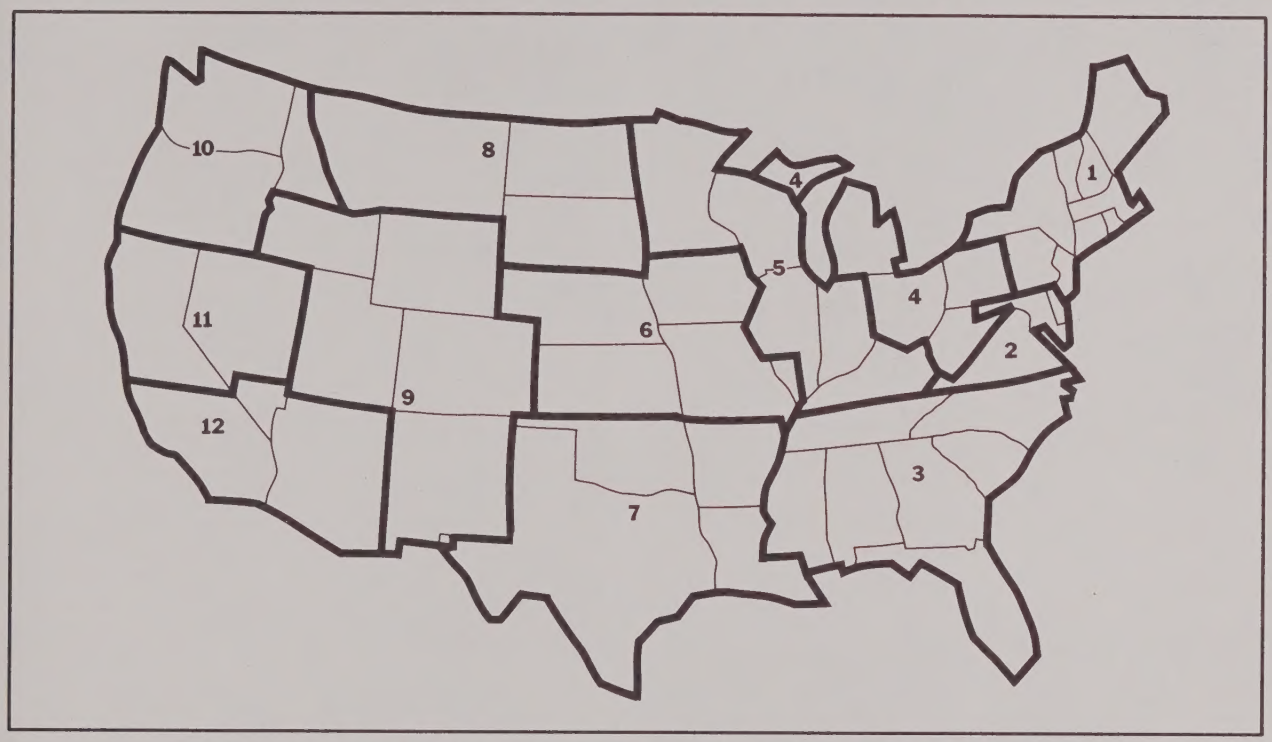


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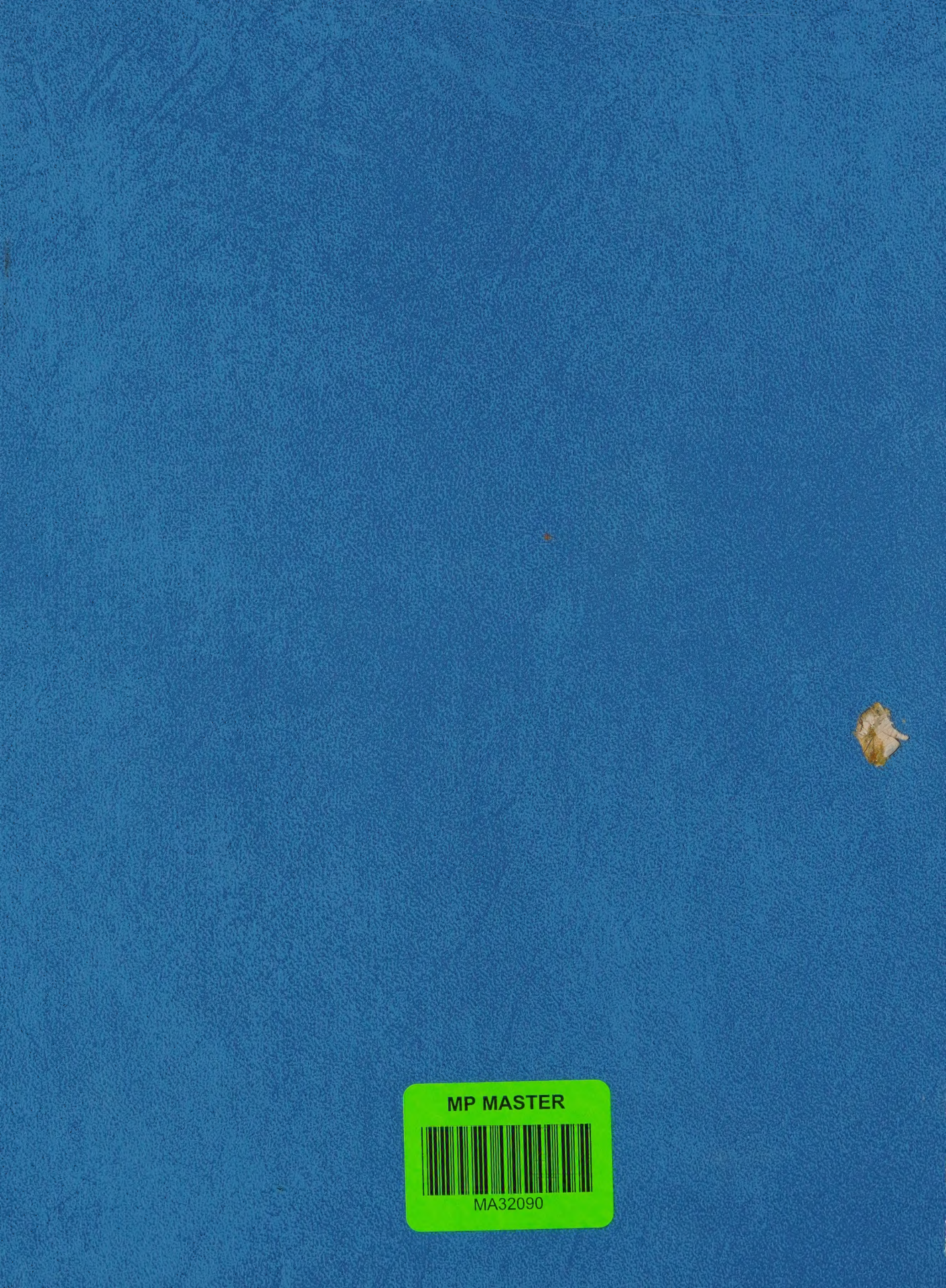
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